International Journal of Current Engineering and Technology
E-ISSN 2277 – 4106, P-ISSN 2347 - 5161

Available at http://inpressco.com/category/ijcet

Research Article

Circuit Design using New Online Testable Reversible CTSG

Aparna. C[Á*] and N.Kirthika[Á]

[Á]Sri Ramakrishna Engineering College, Coimbatore

Accepted 15 April 2014, Available online 23 April 2014, **Vol.4, No.2 (April 2014)**

Abstract

*Reversible logic is emerging and a promising computing paradigm having its applications in low power VLSI design, quantum computing, cryptography, nanotechnology and optical computing. A new 4*4 reversible gate termed OTG (Online Testable Gate) and CTSG are designed suitable for online testability in reversible logic circuits. OTG can also work singly as a reversible full adder with a bare minimum of two garbage outputs. The OTG reversible gate is combined with the existing 4*4 Feynman gate to design online testable reversible circuits. In this paper a 9 CLB compact FPGA is designed using new CTSG logic. The CTSG can be operated as a universal NAND gate. The circuit complexity is reduced compared to the early proposed R1 gate and we can see the reduced delay of the circuits. Since the delay is reduced for the circuit we can say that the circuit can be used for high speed operation. The circuit design has been done using Xilinx ISE Design Suit 13.2.*

Keyword: *reversible logic, online testability, high speed, FPGA,CTSG*

1. Introduction

Reversible computing is a model of computing where the computational process to some extent is reversible, i.e., time-invertible. In a computational model that uses transitions from one state of the abstract machine to another, a necessary condition for reversibility is that the relation of the mapping from states to their successors must be one-to-one. Reversible computing is generally considered an unconventional form of computing. (Landauer, R.1961), in Irreversibility and heat generation in the computing process discussed about heat generation and loss of data in the irreversible process. Landauer's principle asserts that there is a minimum possible amount of energy required to change one bit of information, known as the *Landauer limit*: kT ln 2, where k is the Boltzmann constant (approximately 1.38×10^{-23} J/K), T is the temperature of the circuit in kelvins, and ln 2 is the natural logarithm of 2 (approximately 0.69315).

Theoretically, room temperature computer memory operating at the Landauer limit could be changed at a rate of one billion bits per second with only 2.85 trillionths of a watt of power being expended in the memory media. Modern computers use millions of times as much energy. If no information is erased, computation may in principle be achieved which is thermodynamically reversible, and require no release of heat. This has led to considerable interest in the study of reversible computing.

In Logical Reversibility of Computation (C.H. Bennett 1973) , analyzed more about the reversible concepts which has been introduced by Landauer. In his paper he has been concluded that all operations required in computation could be performed in a reversible manner, thus dissipating no heat. He introduced two types of reversibility

- Logical reversibility
- Physical reversibility.

The advantage reversible computation is it has reduced heat dissipation, higher densities and higher speed. In Online Testable Reversible Logic Circuit Design using NAND Blocks(D.P. Vasudevan et. al.2004), Reversible-Logic Design With Online Testability(D. P. Vasudevan, et. al. 2006) and Fault Testing for Reversible Circuits (K. N. Patel et. al.2004), the online testability of reversible logic is discussed. These papers concluded that the reversible circuit can be tested when it is working in its normal mode.

In this paper we have combined two existing reversible gates. The OTG reversible gate is combined with the existing 4*4 Feynman gate to design online testable reversible circuits. The new gate is known as CTSG. A 9 clb FPGA is designed using new online testable reversible CTSG.

2. OTG and Feynmann Gates

In the era of reversible logic many researchers have introduced different types of reversible gates. The main properties of reversible gates are it should be a n*n gate, it should preserve parity of input and output and must contain less number of garbage outputs. Garbage outputs are the outputs which we are not using as a primary output r as an input to any other circuits.

*Corresponding author: **Aparna. C** is a ME VLSI Design Student and **N.Kirthika** is working as Asst Prof

Recently introduced gates are feynmann gate. The feynmann gate is introduced by a scientist named Feynmann. The feynmann gate is a reversible gate 4*4 gate. It is used for duplicating the signal and the xor operation of all the inputs. Figure 1 shows the Feynamnn gate.

Another reversible gate is OTG. Advantage of OTG is it is online testable gate. OTG can be tested when it is working in the normal mode. We can predict the input from the output of the gate. More over the garbage output is less than that of the previous reversible gates. Figure 2 shows OTG gate.

3. Combination of Feynmann and OTG Gate – CTSG

The reversible feynmann gate online testable OTG gates are combined to work as reversible online testable gate. This gate is called CTSG gate.

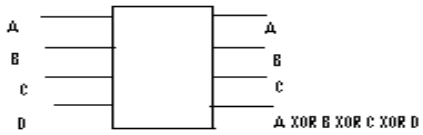

Fig.1. Feynmann Gate

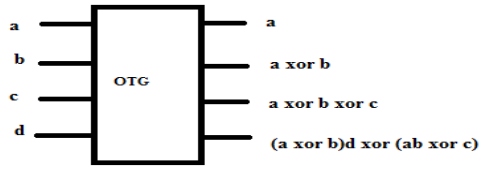

Fig.2. OTG gate

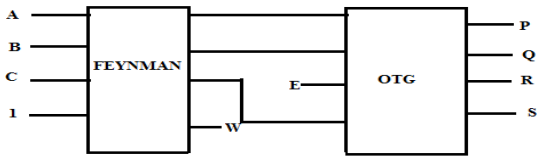

Fig.3. Combination of feynmann and OTG gates.

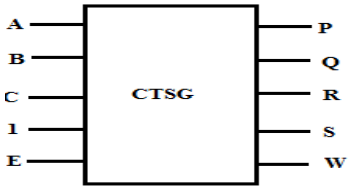

Fig.4. CTSG gate

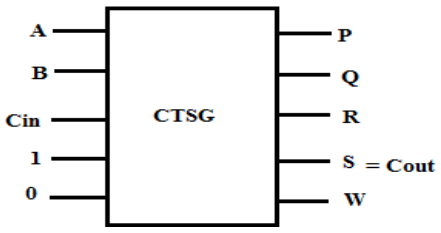

Fig.5. CTSG as full adder

Main advantage of CTSG is we can design AND, NAND and XOR gate by programming the 'C', 'D' and 'E' inputs.
If C => 0,D=>1 and E=>1, then

$$S = \overline{AB} \quad (1)$$

If C=>1, D=>1 and E=>0, then

$$S = AB \quad (2)$$

Output 'Q' of CTSG will directly give the XOR output. Since NAND is a universal gate other gates can be implemented using NAND gate.

4. Proposed Online Testable Reversible FPGA

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing—hence field-programmable. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC) (circuit diagrams were previously used to specify the configuration, as they were for ASICs, but this is increasingly rare). FPGAs contain programmable logic components called logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be wired together—somewhat like many (changeable) logic gates that can be inter-wired in (many) different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. This feature distinguishes FPGAs from Application Specific Integrated Circuits (ASICs), which are custom manufactured for specific design tasks. Although one-time programmable (OTP) FPGAs are available, the dominant types are SRAM based which can be reprogrammed as the design evolves.

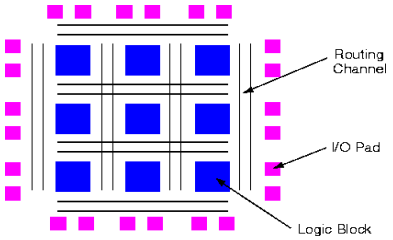

Fig.6. Compact FPGA with 9 CLBs

The CLB is the basic logic unit in a FPGA. Exact numbers and features vary from device to device, but every CLB consists of a configurable switch matrix with 4 or 6 inputs, some selection circuitry (MUXetc.), and flip-flops. The switch matrix is highly flexible and can be configured to

handle combinatorial logic, shift registers or RAM. Configurable Logic Blocks (CLB) are programmable elements inside a Xilinx FPGA.

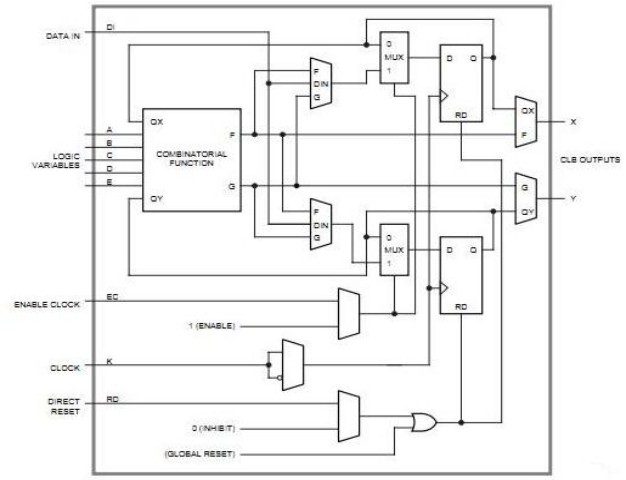

Fig.7. CLB in a Xilinx FPGA

The CLB of a FPGA consists of Look-Up-Tables(LUTs). The LUTs can be programmed to work as desired function. The LUT is the basic component of combinational function unit. Combinational function will have 1 or more LUTs. Each LUT is known as the function generator. In figure 7 the combinational function will have two function generator with outputs F and G. In this project iam going to propose a compact FPGA with 9 CLBs. LUTs in the CLB will act as function generator. In this function generator two functions are programmed. The function generator is a 4 bit function generator, it will process 4 bit data.

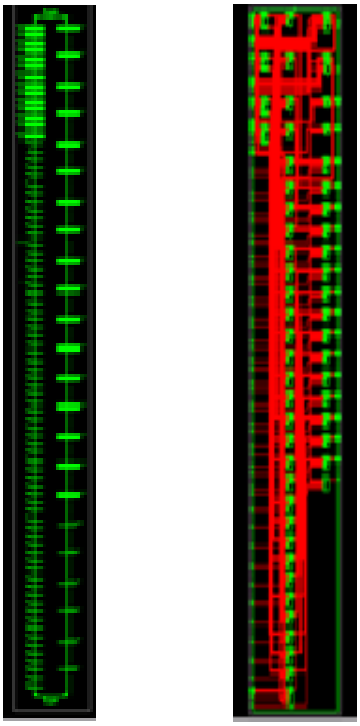

Fig.8(a) **Fig.8(b)**

Fig.8. online testable reversible FPGA

Figure 8 shows the RTL diagram of online testable reversible FPGA. In online testable reversible FPGA there are 9 CLBs. Functions that can be performed by proposed FPGA are ripple carry adder, ripple borrow subtractor, multiplier, decoder, priority encoder, gray to binary and binary to gray code converters, XOR and AND operation, XS3 to BCD and BCD to XS3 converter, comparator, parallel in serial out shift register and binary to BCD converter.

5. Simulation Results

The proposed FPGA has been programmed using VHDL language. Each CLB and associated components are designed using CTSG. Final FPGA has been designed by port mapping the components using structural modeling. Tool used for simulation is Xilinx ISE Design Suit 13.2. Power analysis can be done using Xpower analyzer.

The circuit is analyzed for delay, memory usage. Power is analyzed for internal CLBs only because the tool is providing lesser number of input/output pins than that of actually needed for the FPGA design.

Table I Simulation results of CLBs

	CLB1	CLB2	CLB3	CLB4	CLB5	CLB6	CLB7	CLB8	CLB9
Delay(ns)	11.139	9.047	9.562	11.586	7.226	8.734	11.763	10.302	6.367
Memory(kb)	149476	147420	140452	153572	139236	147420	147327	142308	139236
Power dissipation(mw)	101	104	97	95	82	93	87	83	82

Delays of the circuits are represented in nanoseconds, memory usage in kilobytes and power in mW. From the results we can see that the delays of the circuits are less. So this CTSG design can be used for high speed devices. The circuit can be used for already existing devices for high speed application with small increase in the circuit complexity.

Table II Simulation results of FPGA

	Delay(ns)	Memory(kb)
FPGA	16.474	308960

Table I and II shows the simulation results of proposed CLBs and FPGA.

The concept of reversible logic is reducing the loss of information. By reducing the loss of information we reduce the heat dissipation. The power can be reduced while reducing the heat dissipation of the circuit.

Conclusion

A online testable reversible logic 'CTSG' is introduced. The CTSG is an universal gate. Any logic gate can be designed using CTSG. Since it is a reversible logic the information loss can be reduced. In a ciruit a part of power dissipation is due to the loss of data, using reversible logic the power consumption can be reduced. Also the delay of the CTSG gate is less, so it can be used as a high speed device.

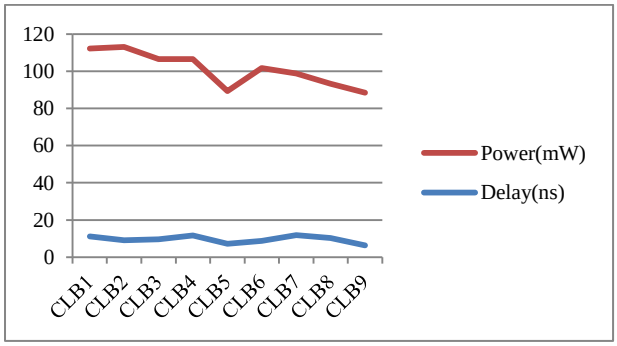

Fig. 9. Power and delay of CLBs

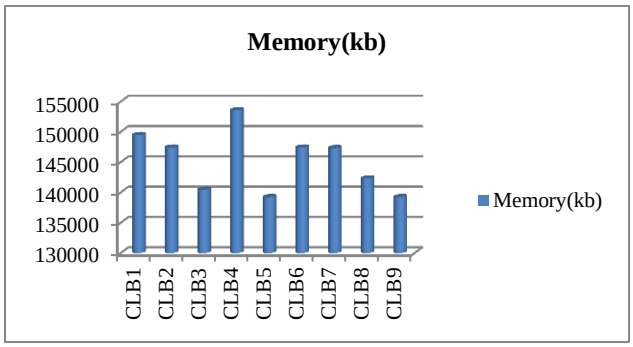

Fig. 10 Memory usage by CLBs

In this paper online testable reversible logic gate 'CTSG' is designed. This CTSG logic is used design an FPGA with 9 CLBs. The design is programmed using VHDL programming with structural modeling. The CLBs are designed and port mapped to design the entire FPGA. The tool used for the design is Xilinx ISE design Suite 13.2, the power is estimated using Xpower analyzer. The delay of the FPGA is obtained as 16.474ns which is very small, it will work as a high speed FPGA.

References

Landauer, R.,(1961). Irreversibility and heat generation in the computingprocess.*IBM J. Res. Develop*., 5: 183-191.

C.H. Bennett (1973) , Logical Reversibility of Computation, *IBM J.Research and Development*, 17, 525

E. Fredkin, T Toffoli (1982) Conservative Logic, *International Journal of Theor. Physics*, vol. 21, nos. 3-4, pp. 219-253.

T. Toffoli.(1980), Reversible Computing, *Tech memo MIT/LCS/TM-151,MIT Lab for Computer Science.*

D.P. Vasudevan,P.K. Lala and J.P. Parkerson,(2004), Online Testable Revrsible Logic Circuit Design using NAND Blocks , *Proc,Symposium on Defect and Fault Tolerance*, pp-324-331.

D. P. Vasudevan, P. K. Lala, J. P Parkerson (2006) Reversible-Logic Design With Online Testability, *IEEE Transactions onInstrumentation and Measurement*, VOL. 55, NO. 2, pp. 406-414

K. N. Patel, J. P. Hayes, and I. L. Markov(2004), ``Fault Testing for Reversible Circuits" , *IEEE Trans. on CAD, 23(8)*, pp. 1220-1230

P.O. Boykin and V.P. Roychowdhury(2005), Reversible fault-tolerant logic Proceedings *International Conference on Dependable Systems and Networks*, (DSN 2005), 28 June-1 July 2005, pp.444-453

LavanyaThunuguntla, BinduMadhavi K, PullaiahT(2005),Designing of Efficient Online Testable Reversible Multiplexers and DeMultiplexers with New Reversible Gate, *IJERA*, ISSN: 2248-9622Vol. 2, Issue 2,Mar-Apr 2012, pp.183-191

Raghava Garipelly, P.Madhu Kiran, A.Santhosh Kumar(2013), A Review on Reversible Logic Gates and their Implementation, *IJETAE*,ISSN 2250-2459, ISO 9001:2008,Volume 3, Issue 3, March 2013