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Research Article

Investigation of Fully Depleted SOI and MOSFET Characteristics

Towhid Adnan Chowdhury*

Assistant Professor, Department of Electrical & Electronic Engineering, Ahsanullah University of Science & Technology, Dhaka,Bangladesh.

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Abstract

The electrical characteristics of n-channel fully depleted silicon on insulator (FDSOI) and metal oxide semiconductor field effect transistor (MOSFET) are investigated in this paper. Both transistors are compared in terms of electrical characteristics which are the threshold voltage, subthreshold slope, on-state current and leakage current. Silvaco TCAD tools are used for simulating both MOSFET and FDSOI MOSFETs. Based on the results, it can be concluded that FDSOI MOSFET outperforms MOSFET.

Keywords: *Silicon on Insulator, Fully-Depleted, Subthreshold Slope, Leakage Current, Silvaco.*

1. Introduction

Miniaturization of device area and increased device packing densities meet the need for high performance circuit today [1,2]. The International Technology Roadmap of Semiconductors (ITRS)[3] applies aggressive scaling trends for the gate length (*LG*) and equivalent gate oxide thickness (EOT) to meet the requirement of a 17% annual reduction of the intrinsic switching delay for high-performance transistors. Due to scaling down industry is facing problem due to short channel effect (SCE) using bulk MOSFET[4]. Silicon on Insulator (SOI) is considered as a promising alternative over conventional bulk device due to its benefits of decreased silicon geometries. Silicon on Insulator (SOI) technology possesses many benefits over bulk silicon technology, such as excellent subthreshold slope, elimination of latch up, resistance to radiation and the reduction of parasitic capacitance [5]. Hence, it is preferred for high-temperature, high-speed and low-power microelectronic devices. In SOI MOS devices a buried insulating thin layer usually made of silicon dioxide is employed to electrically insulate the devices from the bulk of the semiconductor. Silicon on insulator (SOI) is available in two basic types, partially (PD) and Fully (FD) Depleted. These are distinguished physically by the silicon thickness on the insulator. Both of them are now attractive for IC production. PD material has a silicon film thickness greater than about 150 nm. Its depletion region does not pass through the entire body region. PD-SOI is easier to fabricate than FD-SOI because of its thicker substrate [6]. The kink effect is present in PD SOI devices which is not visible in FD SOI devices [7].

*Corresponding author's ORCID ID: 0000-0000-0000-0000
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For fully-depleted SOI devices, the thickness of silicon film is about less than 100nm. So the channel is completely depleted of the majority carriers due to thinner top silicon layer. The benefit of FD SOI MOSFET includes better short channel behaviour and the elimination of the floating-body effect. This paper presents comparison between MOSFET and fully depleted SOI devices in terms of electrical characteristics which are threshold voltage, subthreshold slope, on-state current and leakage current. TCAD Silvaco software was used for simulation study of SOI devices. Simulation results revealed that the electrical characteristics such as threshold voltage, subthreshold slope and on-state current of fully depleted SOI outperformed than that of MOSFET devices.

Methodology

To study the electrical parameters of FD SOI and MOSFET a schematic cross-sectional view of the MOSFET and FD SOI, shown in Fig.1(a) and (b), is simulated using Silvaco TCAD device simulator. 120 nm and 80 nm gate length FD SOI devices are compared with MOS devices.For the 120 nm gate length FD SOI device, gate oxide thickness is of 3nm,source and drain length is of 120 nm, silicon film thickness is of 48 nm,buried oxide thickness of 160 nm,p-substrate is of 100nm. We assumed light channel doping concentration (1×10^{18} cm^{-3}) to avoid degrading of carrier mobility and more Vt variations. The doping concentration of source/drain region is kept at 1×10^{19} cm^{-3}. For the 80 nm gate length FD SOI device, gate oxide thickness is of 2 nm,source and drain length is of 80 nm, silicon film thickness is of 32 nm,buried oxide thickness of 100 nm,p-substrate is of 70 nm. The doping

concentration of source/drain region is kept at 1×10^{20} cm^{-3}. For both 120 nm and 80 nm gate length MOSFET structure, only the buried oxide is replaced by p-substrate of same thickness of the FD SOI structure. The channel, source and drain doping concentration for MOS was same as that used for FD SOI. Shockley-Read-Hall recombination, field-dependent mobility model and impact ionization model from Selberherr [8] is used for the simulation. Numeric methods used for simulation are Newton methods. We assumed n channel device.

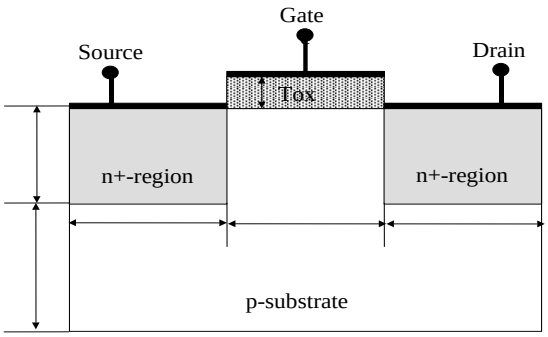

Fig.1.(a) Schematic view of n- channel MOSFET

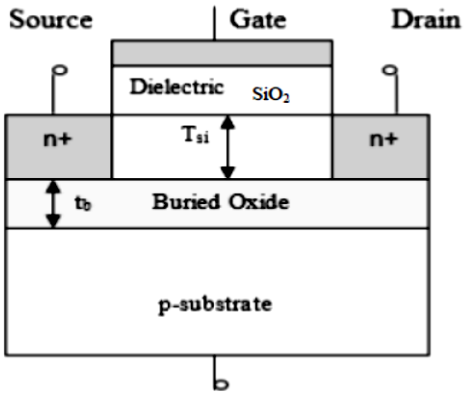

Fig.1.(b) Schematic view of FD SOI MOSFET

Result and discussion

The n-channel MOS and FDSOI MOSFET has been investigated in terms of electrical parameters by simulation results obtained using Silvaco TCAD simulation software. Atlas syntax is used to create SOI structures and TonyPlot is used to display simulation results. Fig.2(a), Fig.2(b),Fig.3(a) and Fig.3(b) shows the structural view of simulated 120 nm gate length MOSFET, structural view of simulated 120 nm gate length FD SOI MOSFET, doping profile view of simulated 120 nm gate length MOSFET and doping profile view of simulated 120 nm gate length FD SOI MOSFET respectively. Fig.4(a), Fig.4(b),Fig.5(a) and Fig.5(b) shows the structural view of simulated 80 nm gate length MOSFET, structural view of simulated 80 nm gate length FD SOI MOSFET, doping profile view of simulated 80 nm gate length MOSFET and doping profile view of simulated 80 nm gate length FD SOI MOSFET respectively.

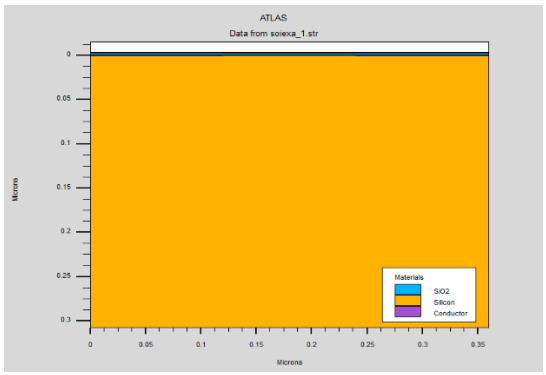

Fig.2(a) Simulated structure of 120 nm gate length MOSFET

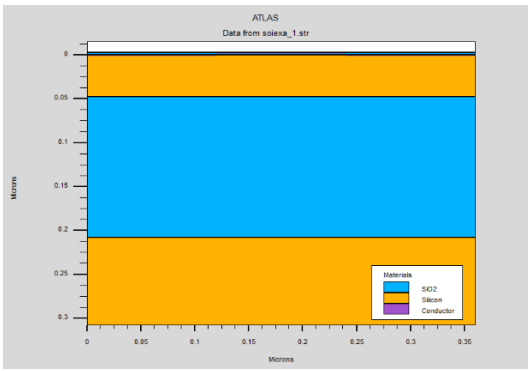

Fig.2(b). Simulated structure of 120 nm gate length FD SOI MOSFET

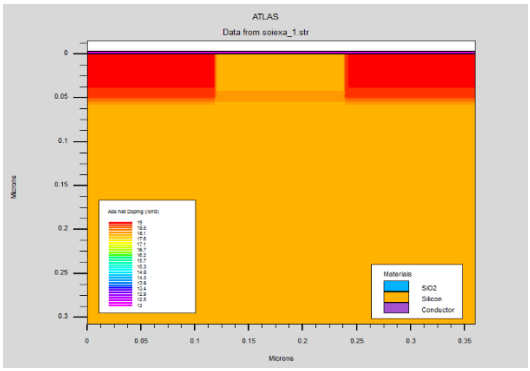

Fig.3(a) Doping profile of 120 nm gate length MOSFET

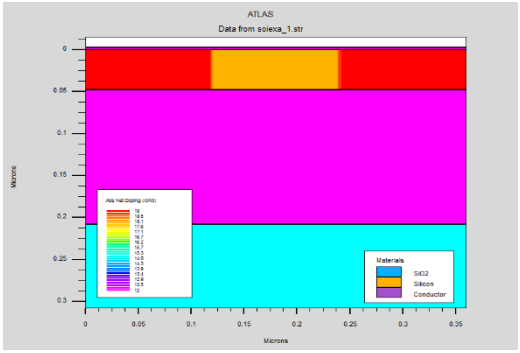

Fig.3(b) Doping profile of 120 nm gate length FD SOI MOSFET

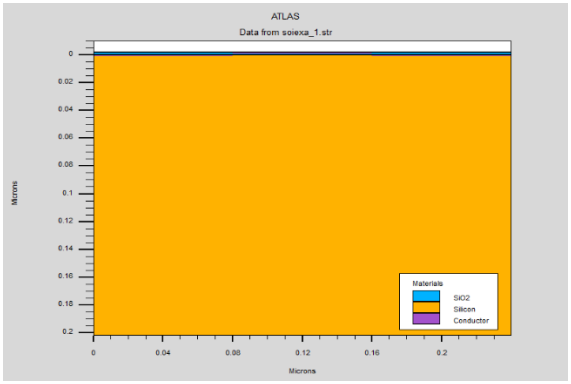

Fig.4(a) Simulated structure of 80 nm gate length MOSFET

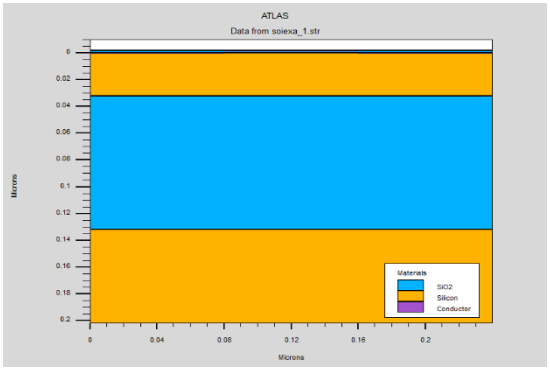

Fig.4(b) Simulated structure of 80 nm gate length FD SOI MOSFET

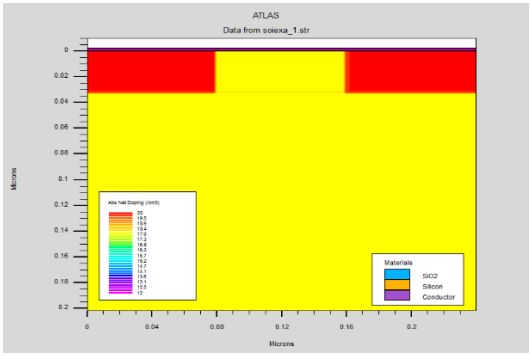

Fig.5(a) Doping profile of 80 nm gate length MOSFET

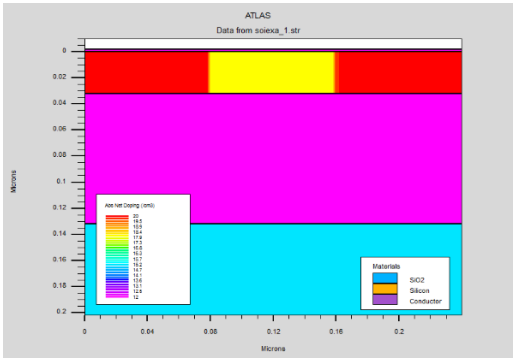

Fig.5(b) Doping profile of 80 nm gate length FD SOI MOSFET

The electrical parameters obtained for FD SOI and MOS at different gate length is shown in Table 1 and Table 2.

Table 1. Comparison of the electrical characteristics between FD SOI n-MOSFET with n-MOSFET at 120 nm gate length

Parameters	NMOS	FD SOI
Threshold Voltage,Vth(V)	0.345356 V	0.30355 V
Subthreshold slope(mV/dec)	82.74	79.14
On-state current,I_{on}(A)	0.000143127	0.000253829
Leakage current,I_{off}(pA)	31.4162	135.27

Table 2. Comparison of the electrical characteristics between FD SOI n-MOSFET with n-MOSFET at 80 nm gate length

Parameters	NMOS	FD SOI
Threshold Voltage,Vth(V)	0.211319 V	0.091869 V
Subthreshold slope(mV/dec)	83.39	73.48
On-state current,I_{on}(A)	0.000690017	0.000879956
Leakage current,I_{off}(μA)	0.037	0.39

The Ids/Vgs characteristics comparison between n-MOSFET and FDSOI n-MOSFET is shown in Fig.6 & Fig.7. Smaller threshold voltage satisfies high performance of device with technology scaling [9]. The threshold voltage for MOS and FDSOI are 0.34535 V and 0.30355 V respectively as extracted from simulation results for 120 nm gate length. The voltage between the gate and source needed to turn on the MOSFET is defined as MOSFET gate threshold voltage, Vgs(th)[10]. FDSOI MOSFET will trigger when the threshold voltage is equal to 0.091869 V while MOSFET will trigger when threshold voltage is equal to 0.211319 V for 80 nm gate length.. It can be concluded that the threshold voltage of n-MOSFET is larger than FDSOI n-MOSFET from the results for both the gate lengths. FDSOI devices gained highest speed of operation and power reduction. A steeper subthreshold slope and threshold voltage reduction allows fast switching of FD SOI MOSFET [11].FD SOI MOSFET of smaller gate length has lower threshold voltage and so faster switching speed.

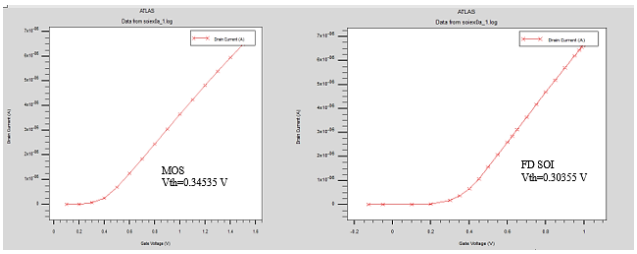

Fig. 6. Comparison of Ids/Vgs characteristics between 120 nm gate length MOS and FDSOI N-MOSFET

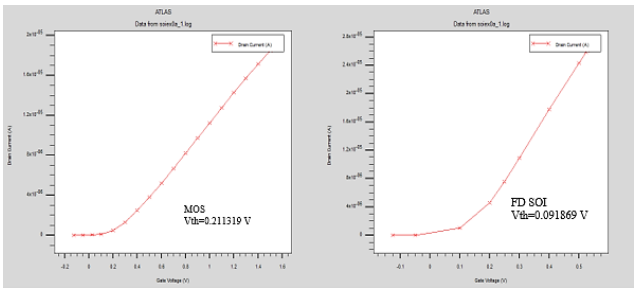

Fig. 7. Comparison of Ids/Vgs characteristics between 80 nm gate length MOS and FDSOI

Subthreshold slope is a measure of how quickly the transistor can be turned on/off. The smaller subthreshold value indicates the device rapidly switches from off to on state. Comparison of subthreshold slope between MOS and FD SOI is shown in Fig.8 & Fig.9. The subthreshold slope for MOS and FDSOI are 82.74 mV/dec and 79.14 mV/dec respectively for 120 nm gate length. For the 80 nm gate length, the subthreshold slope for MOS and FDSOI are 83.39 mV/dec and 73.48 mV/dec respectively. For both the case, the smaller subthreshold slope of FD SOI indicates high speed. As device size shrinks, the subthreshold slope of FD SOI decreases indicating fast switching.

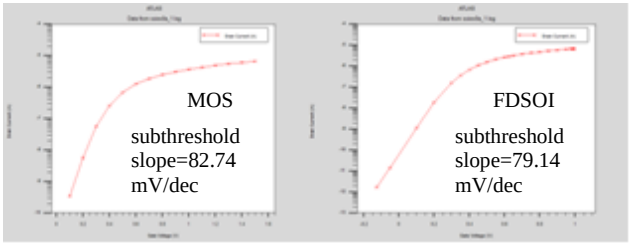

Fig. 8. Comparison of subthreshold slope characteristics between 120 nm gate length MOS and FDSOI N-MOSFET

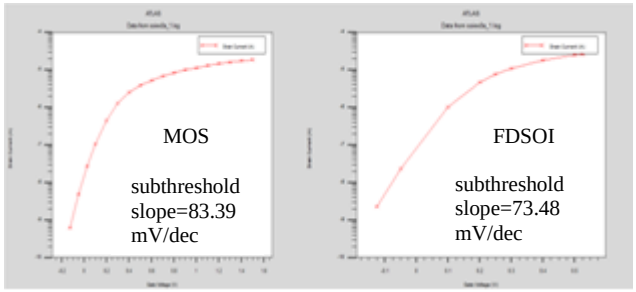

Fig. 9. Comparison of subthreshold slope characteristics between 80 nm gate length MOS and FDSOI N-MOSFET

A high on-state current (I_{on}) helps to increase the operating speed of the device. The on-state current for MOS and FDSOI are 0.000143127 A and 0.000253829 A respectively for 120 nm gate length. For the 80 nm gate length, the on-state current for MOS and FDSOI are 0.000690017 A and 0.000879956 A respectively. For both the case, the higher on-state current of FD SOI indicates high speed. As gate length decreases, the on-state current of FD SOI increases indicating fast switching.

The leakage current (Ioff) becomes lesser with the increment of threshold voltage [12]. The smaller the threshold voltage, the higher the leakage current. MOSFET failure occurs when leakage current flows excessively. Comparing the simulation results of MOS and FDSOI it can be decided that the leakage current in MOS is lesser. High leakage current of semiconductor device is caused due to ionizing radiations by the electron-hole pair generation. The buried oxide layer in SOI helps to eliminate the radiation effects in devices[13]. Static power dissipation is caused by leakage current and when input transition is absent leakage power dissipation is contributed by current flow [14]. Static power dissipation will be small if leakage current is smaller. Thus, from the simulation results the MOS will have a smaller static power dissipation than FDSOI.As gate length decreases, leakage current in FD SOI increases due to reduction in threshold voltage.

The comparison of electrical parameters of fully-depleted SOI n-MOSFET at different gate length is shown in Table 3.

Table 3. The extracted electrical parameters of fully-depleted SOI n-MOSFET at different gate length

Parameters	120 nm Gate Length	80 nm Gate Length
Threshold Voltage,Vth(V)	0.30355 V	0.091869 V
Subthreshold slope(mV/dec)	79.14	73.48
On-state current,I_{on}(A)	0.000253829	0.000879956
Leakage current,I_{off}(μA)	0.000135	0.39

Conclusion

MOSFET and FDSOI has been compared in terms of electrical characteristics using Silvaco T-CAD Simulator. From transfer characteristics it is found that threshold voltage of FDSOI is lower compared to MOSFET which allows a lower power consumption. The smaller subthreshold slope and higher on-state current of FD SOI compared to MOSFET ensures higher switching speed. MOSFET can ensure a low static power dissipation as leakage current is small compared to FD SOI. Based on the results obtained, FD SOI displays superior performance compared to MOSFET. When scaling down continues in FD SOI devices, both threshold voltage and subthreshold slope decreases and on-state current increases as found from simulation results.

References

[1] R. Dennard, F. H. Gaensslen, V. L. Rideout, E. Bassous, and A. LeBlanc,"Design of ion-implanted MOSFETs with very small

physical dimensions," IEEE Journal of Solid-State Circuits, vol. SSC-9, no. 5, pp. 256–268,Oct. 1974.
[2] G. Baccarani, M. R. Wordeman, and R. Dennard, "Generalized scaling theory and its application to a 1/4 micrometer MOSFET design," IEEE Transactions on Electron Devices, vol. ED-31, no. 4, pp. 452–462, Apr. 1984.
[3] International Technology Roadmap for Semiconductors, 2005 ed.[Online]. Available: http://www.itrs.net
[4] K. Suzuki, Y. Tosaka, and T. Sugii, "Analytical threshold voltage model for short channel double-gate SOI MOSFETs,"IEEE Transactions on Electron Devices, vol. 43, no. 7, pp. 1166– 1168, Jul. 1996.
[5] M. Yoshimi, H. Hazama, M. Takahashi, S. Kambayashi, T. Wada, K.Kato, and H. Tango, "Two-dimensional simulation and measurement of high-performance MOSFETs made on a very thin SOI film," IEEE Transactions on Electron Devices, vol. 36, pp. 493–503, Mar. 1989.
[6]G. Shahidi et. at., "A Room Temperacure O.l μm CMOS on SOI," IEEE Transactions on Electron Devices, vol. 41, pp. 2405 – 2412, Dec. 1994.
[7] K. Bernstein and N.J. Rohrer, "SOI Circuit Design Concepts,"Kluwer Academic Publishers, 2000.
[8] ATLAS User's Manual Device Simulation Software, Silvaco International, Santa Clara, Calif., USA, 2004.
[9]A. Verma, A. Mishra, A. Singh and A. Agrawal, "Effect of threshold voltage on various CMOS performance parameter," International Journal of Engineering Research and Applications, vol.4(4), pp.21–28, 2014.
[10] N.Gupta, J.K.B.Patel and A.K.Raghav,"An accurate 2D Analytical Model for Transconductance-to-Drain Current ratio (gm/Id) for a Dual-Halo Dual-Dielectric Triple-Material Cylindrical-Gate–All-Around (DH-DD-TM-CGAA) MOSFETs,"International Journal of Engineering, vol. 31(7),pp. 1038-1043,July 2018.
[11] B. Vandana, "Study of floating body effect in SOI technology," International Journal of Modern Engineering Research ,vol.3(3), 1817–1824, 2013.
[12] S. Cristoloveanu and S. Li,"Electrical Characterization of Silicon-on-insulator Materials and Devices," Springer US,2014.
[13] J. Gupta, S. Choudhary and B. Prasad, "Comparative study of conventional and SOI inverters using Silvaco TCAD tool," Advanced Research in Electrical and Electronic Engineering, vol.1(3), pp.61–65, 2014.
[14] S. K. Singh, B. K. Kaushik, D. S. Chauhan and S. Kumar, "Reduction of subthreshold leakage current in MOS transistors," World Applied Sciences Journal, vol.25(3), pp.446–450, 2013.