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Research Article

SEPIC converter of Automatic Power Factor Correction by improved traditional linear control

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Abstract

With increasing using of nonlinear electronic equipment at a wide range, total harmonics distortion (THD) in the line current has grown to be a considerable problem. The methods that include reducing harmonics in line current and power factor correction are required. Therefore, the essential target of this proposed work is to reduce the harmonics produced in the line current and improve the power quality of the load by the output voltage regulation and power factor correction (PFC). This paper presents a Single-Ended Primary Inductance Converter (SEPIC) at Discontinuous Conduction Mode (DCM) for automatic power factor Correction (APFC). The SEPIC converter is modeling by utilizing Current Injected Equivalent Circuit Approach (CIECA). The control system is applied by traditional linear control (TLC). The TLC has been modified by an optimization algorithm (OA) and adds an (inner or current). The proposed design of SEPIC-PFC is implemented by MATLAB and Simulink. According to the simulated dynamic behavior results, a unity power factor and 15% of total harmonics distortion (THD) reduction have been obtained comparing with previous work. Besides, a regulated DC output voltage has been achieved. The proposed control system has a low overshoot, small settling time, and steady-state error close to zero.

Keywords: *Single-Ended Primary Inductance Converter (SEPIC); Discontinuous Conduction Mode (DCM); Automatic power factor Correction APFC; Current Injected Equivalent Circuit Approach (CIECA); Traditional Linear Control (TLC); Power Factor Correction (PFC); Total Harmonics Distortion (THD).*

1. Introduction

For a hundred years, people have benefited from the electric power system in every aspect. Our community today has been fully perceiving to protect the environment of our planet live. Commended worried about the "dirty" environment in the energy system was not drawn up until the mid-1980s [1-3]. The rapid development of power electronic systems and semiconductor devices has grown and widened to include a modern and enormous range of applications. Such interfaces of energy electronic circuits like '' switched-mode power supplies'' (SMPS); has nonlinear conduct, are caused to drag distorted line current and will create high harmonic distortion resulting in low power factor [4]. Therefore, the rising of power quality is progressively desired for the power supply systems to conform to international standards [5]. There are many ways to improve the power factor, one of which is the switched source, which has the advantage of using a DC-DC converter to create a power factor correction (PFC) system.

As illustrated in Fig. 1, this technique produces a realizable DC-DC converter to construct almost perfect rectifiers of regulating voltage or current and thus power. The switched-mode topologies have also been introduced in the literature [4,6-9] and each one is preferred over the other depending on their energy level and application. . However, the topologies of Single-Ended Primary Inductance Converter (SEPIC) had been beaded of the disadvantages introduced by the popular adapter (boost converter) like the implementing of insulation in between input and output. Therefore, SEPIC becomes a good option in PFC applications. Most recently, SEPIC converters have been involved in great interest of recent applications, particularly that include renewable power such as LED (light-emitting diode) [10-12], battery chargers [13], and photovoltaics (PVs) systems [14]. The classical control technique for PFC converter is illustrated in [15], the main control techniques are inspected to realize sinusoidal input currents and reviewed and analyzing. Therefore, many methods have been developed for determining the parameters of PI controllers Like the Ziegler-Nichols method and Cohen-Coon method [16].

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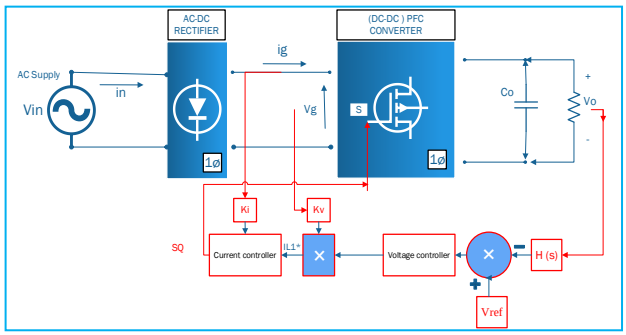


Fig. 1: Diagram of the DC-rectification and a PFC stage with the control system.

In this work, analysis, design, and modeling of the SEPIC is presented based on the discontinuous conduction mode (DCM) and a small-signal model by the current injected equivalent circuit approach (CIECA) technique. Moreover, the control technique improves the operation of the modified traditional linear control (M-TLC) based on an optimization algorithm and modified loop control. The performance and control of SEPIC-PFC are tested using MATLAB & Simulink, which analyzes the PF on the AC side, THD of the input current, and the DC side voltage regulation.

The paper is prearranged as follows. Sections 2 and 3 present the analysis, design, and modeling for the converter in DCM. The description of the control technique that is applied to the SEPIC-PFC is shown in Section 4. Section 5 demonstrates and discusses the main simulation results. Finally, Section 6 includes conclusions and contributions.

2. SEPIC-PFC System Description

The first step of design SEPIC-PFC is the calculation of the reactive components for the power circuit of the converter at discontinuous conduction mode (DCM) [18]. Fig. 2 illustrates the circuit diagram of SEPIC-PFC, where the values of reactive components (L1, L2, C1, and C2) for SEPIC in DCM is shown in Appendix A. A SEPIC converter is displayed in Fig. 3. Which is used for converting the AC input signal to a DC signal. Fig. 3 (a) includes a MOSFET switch (Q), a diode (D), two capacitors (C_1 and C_2), and two inductors (L_1 & L_2). The resistor, R is regarded as a constant load, and the current source, I_z, models the load current. The resistors r_{C1},r_{C2}, r_{L1}, and r_{L2}, are equivalent series resistances (ESRs) of the capacitors and inductors, respectively. Their values are generally so small compared with R. In the idealistic converter, ESRs are zero. At DCM, the converter has two cases as shown in Fig.4 [17]. The first state is when Q switched ON as shown in Fig. 3(b) over the duty period (dT), into which L_1 charged by the source V_g, whereas L_2 is charged by the capacitor C_1, therefore, i_{L1} and i_{L2} are growing linearly. In the second state, Q is switched OFF as shown in (Fig.3 (c)), during the period, $((1-d)T)$, L_1 and L_2 are in the discharge phase; therefore L_1 and L_2 relieve the energy stored in the capacitance and the load respectively, hence, i_{L1} and i_{L2} reduced linearly.

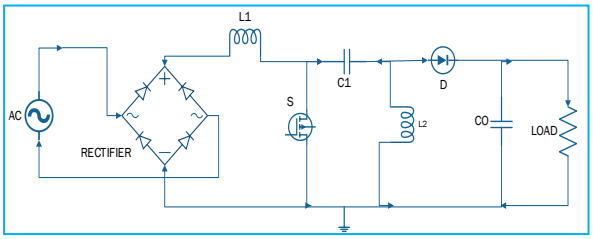


Fig. 4: Designing of SEPIC-PFC

The output voltage V_o is a DC voltage that contains a small ripple because of the switching action. To idealistic SEPIC converter, the relation between V_o *and* V_g is [17]:

$$M = \frac{V_o}{V_g} = \frac{d}{(1-d)} \qquad (1)$$

where M is the voltage conversion ratio and d is the duty cycle. It can be seen that V_o could be larger or smaller than V_g, depending on the duty cycle.

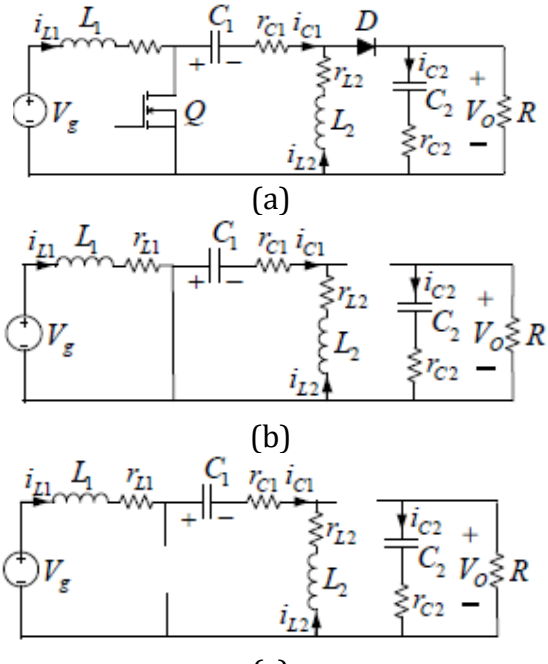


Fig. 3. Operation of SEPIC in DCM☹a) SEPIC converter, (b) SEPIC converter during the first state d_1T, and (c) SEPIC converter during the second state d_2T [21].

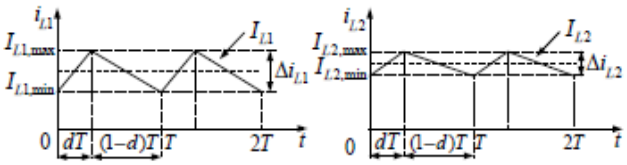


Fig. 4. Current waveforms [17].

After the principles working of the SEPIC has been explained, the model of dc-dc switching power converter uses an approach called the "current injected equivalent circuit approach" (CIECA) [18]. The principle

for this approach with outcomes from a set of equations, which fully describe the input/output characteristic. The small-signal model for SEPIC is shown in Fig. 5. The benefits of CIECA are:

1. If the converter operates both in (CCM) or DCM, the design is very clear and simple.
2. An equivalent circuit is a product for a true converter in the CIECA Model.

A small-signal model can be obtained by using the CIECA approach [19]. The small-signal perturbations will be applied to both input and output average currents:

$$i_{in} = I_{in}\sin(wt) \quad (3)$$

$$I_o = \frac{V_{in}^2 D^2 T_s}{4L_{eq} v_o} \quad (4)$$

$$I_{in} = \frac{V_{in} D^2 T_s}{2L_{eq}} \quad (5)$$

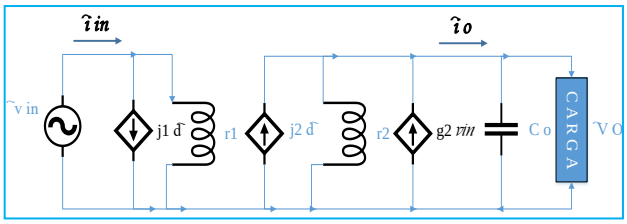


Fig. 5: The small signal of the SEPIC-PFC equivalent circuit

The equivalent electric circuit described by (6) and (8) is shown in Fig. 5. From the equivalent circuit, the transfer function for the particular application can be found.

$$\hat{\imath}_o = j_2\hat{d} + g_2\hat{v} - \frac{1}{r_2}\hat{v} \quad (6)$$

Where

$$g_2 = \frac{\overline{V_1}\,\overline{D^2}T_s}{\overline{V}\,2L_{eq}},\ j_2 = \frac{\overline{V_1}^2\,\overline{D}T_s}{\overline{V}\,2L_{eq}} \text{ and } r_2 = \frac{\overline{V}}{I_o} \quad (7)$$

Repeat the procedure for equation (5) results well are:

$$\hat{\imath}_1 = j_1\hat{d} + \frac{1}{r_1}\hat{v}_1 \quad (8)$$

Where:

$$g_1 = \frac{\overline{V_1}\,\overline{D}T_s}{L_{eq}},\ r_1 = \frac{2L_{eq}}{\overline{D^2}T_s} \quad (9)$$

Therefore, the equivalent circuit identified by (6) and (7) is depicted in Fig. 5, the equivalent circuit can extract the transfer function for the output voltage with the duty cycle:

$$G_{dv}(s) = \frac{j_2}{C_o S + (\frac{1}{r_2} + \frac{1}{R_L})} \quad (10)$$

3. Control Strategies

The control system is a major part of the whole system. The classic control system of the PFC converters was developed. The main purpose is to have to make a good controller for the ability to introduce the optimum performance of the plant system. The strategy of control relies on the traditional approach by the unit controller (PI). The modified process has been implemented by an optimization algorithm (OA) and adds an (inner or current) loop. In this strategy, there are two loop modes; the OA applies to obtain a better result, which has the best performance in between, as follows:

1. The Voltage loop mode.
2. Modified loops mode (Voltage and Current).

4. Optimization Algorithm (OA)

A fundamental step in designing the OA is to have the design requirements. The performance parameters for the controller design is as follows:

1. Settling time is less or equal to 3 seconds.
2. Peak overshoot is less or equal to 10%.
3. Steady-state error is less or equal to 1%.

After considering the performance requirements, the following steps were taken for designing a PI controller to Optimization of Proportional-Gain (K_p) and the location of Zero:

1. Give a specified range of proportional gain value (K_p).
2. Estimate the expected location of zero by giving a specific range of values for the expected zero location (a).
3. Define the system transfer function that carries the characteristics to be controlled.
4. Define the transfer function of the PI controller.
5. Build the transfer function for a closed-loop system.
6. Get on the step response for the closed-loop system.
7. Check the wanted specifications are satisfied.
8. Add the conditions according to the required specifications, and show the initial solutions relative to the proportional gain (K_p) value and the zero position (a).
9. Find the optimum values of (K_p and a) for the control unit parameters that obtain the desired specifications.
10. Via applying the optimum values for (K_p and a), connect the controller with the plant system.
11. If the specifications are satisfied, determine the value of integral gain (K_i) using the following formula:

$$K_i = K_p * a \quad (11)$$

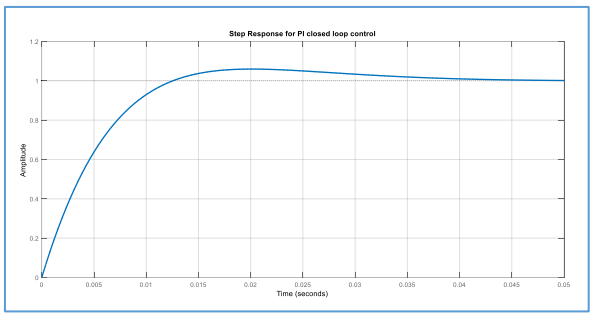
12. Finally, enter the exit command.

As a result, the performance of OA is the transfer function of the PI controller $G_c(s)$ as

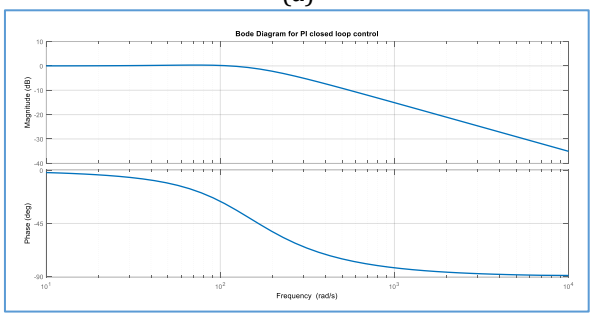
$$G_c(s) = \frac{0.01\,(s+100)}{s} \quad (12)$$

The step response and bode plot response for closed loop system is illustrated in Fig.6 and it is performance parameters, which is satisfies the desired system requirements as follow:

- Rise time (sec) = (0.00914), Settling time (sec) = (0.0351),
- Maximum overshooting = 4.7% and Final value = (1).
- Peak margin (dB) = (0.218) at frequency (rad/s) = 61.8
- Phase margin (deg) = (154) at frequency (rad/s) = 96.4



(a)



(b)

Fig. 6: Characteristics of closed-loop system for (a) step response and (b) bode plot diagram.

5. The Voltage loop mode

The voltage proportional-integral PWM controller is modified by a utilized optimization algorithm. Fig. 7 illustrates the voltage loop mode. The PI controller and the SEPIC converter are replaced by their respective transfer functions respectively $G_c(s)$ and $G_{vd}(s)$, the transfer function $G_{vd}(s)$ is imputed to the ratio between the output voltage and the duty cycle. The other elements identified as the value of the triangular wave VM for (PWM) and voltage sensor gain $H(s)$. The PI modified controller depends on clarifying the transfer function T(s), that introduced by:

$$T(s) = \frac{H(s)G_c(s)G_{dv}(s)}{VM} \quad (13)$$

The transfer function for the reduced Gdv transfer function according to (9) is:

$$G_{dv}(s) = \frac{282.25}{0.016s + 1} \quad (14)$$

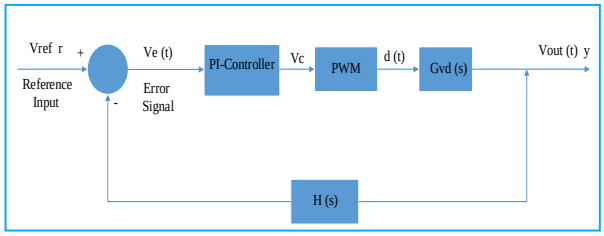


Fig. 7: Voltage Loop Control.

Thus, the steady-state control system performance had evaluated for Voltage loop mode is illustrate in Fig.8. Can say that for the following performance criteria selected` for controller design had been achieving.

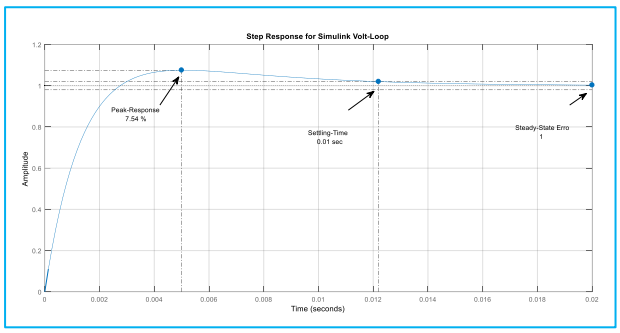


Fig8: The Steady-state response.

The target from this mode is to get the regulation of voltage on the DC side and high PF with reducing THD for SEPIC-PFC. Although it has been achieved the total harmonic distortion (THD) but it remains high and that not useful.

6. Modified loops mode (Voltage and Current)

The modulation of the loop is the solution to overcome the defects of voltage loop mode. By inserting an extra loop, the inner loop or current, which is designed for ensuring the formation of the iL_1 input current wave and then reducing THD. The control unit is illustrated in Fig.9. It is formed from two consecutive loops. The current loop is formed to reshaping the input current wave. The voltage loop is the purpose to regulate the DC output voltage plus to stable it about the desired set point. Besides, the controller is using a single linear proportional-integral (PI) instead of two controllers with PWM are designed to act on controlling the two loops for voltage and current.

The inner loop contains two important gains controlling the input current (i_{L1}) and voltage (V_g) signals of the converter. K_i and K_v are the scaling gain. The K_i of the current signal work on reduces THD and K_v the gain of the voltage signals regulates the DC voltage, respectively. Where both operate opposite to the other, or in other words the two cannot be adjusted

at the same time to get the voltage regulation and the low of theTHD. If tried to adjust the $K_i$to have a lowTHD, resulting would get poor or no regulation and vice versa. Therefore, this is done by tuning these scaling gains, as a result, the control process will be completed and ensure wave formation of DC input current, and thus to improve the power factor with regulates the DC voltage. The steady-state control system performance was evaluated for modifying voltage and current loop mode is illustrate in Fig.10, hence, as see that the required performance was achieved.

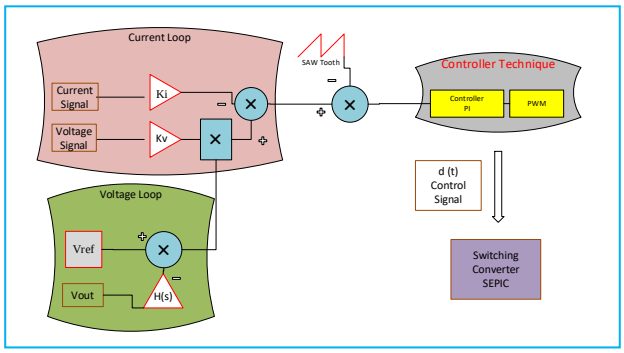


Fig. 9: Block diagram for voltage and current loops control.

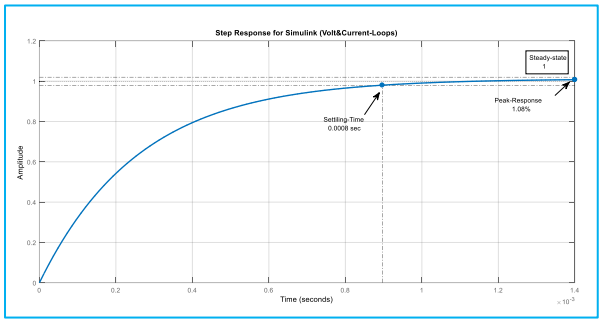


Fig.10: Steady-state response

6. Results and Discussion

The performance of the system was testing before implementing the improved process. Fig.11 is shown the dynamic behavior of the SEPIC-PFC. It is noticed that the output voltage of the DC is not regulated and the harmonic distortion of the input current is high. Therefore, this is not useful and is not practical at all. By applying the voltage loop mode control, the dynamic conduct is illustrated in Fig. 12. The performance of the system is capable to regulate the output voltage. Fig.13 shows the harmonics bar and indicate to achieve low THD. As result, the SEPIC-PFC has a high PF, low harmonic contented in AC and the DC output is regulated. Although the improvement process has been done it can say that the development of the linear technique indicates a little progression. Nevertheless, when the modified control inner loop is implemented, the dynamic behavior of the SEPIC-PFC is shown in Fig. 13. The voltage and current are with the same phase with a little disturbance time at the start. During this time, the system will be stable with small distortion. A high-power factor has been achieved and better regulation DC output voltage. Fig 14 shows the harmonics bar which is decreased in THD as compared with [2, 5].

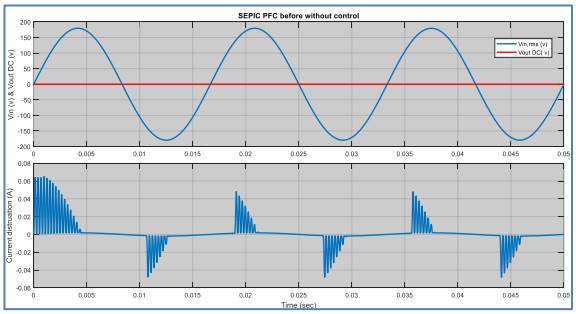


Fig. 11: Dynamic behavior of the SEPIC-PFC before applying the control unit

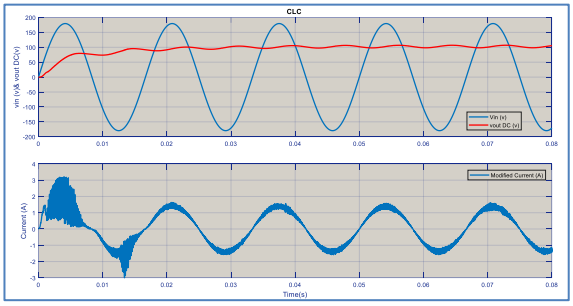


Fig. 12: Dynamic behavior for SEPIC-PFC for M-TLC (Voltage–Loop) Control

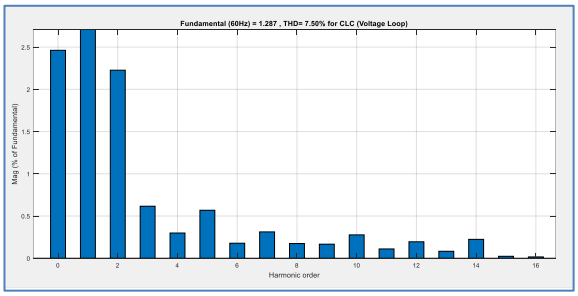


Fig. 13: The harmonics bar for SEPIC-PFC for M-TLC (Voltage–Loop) Control

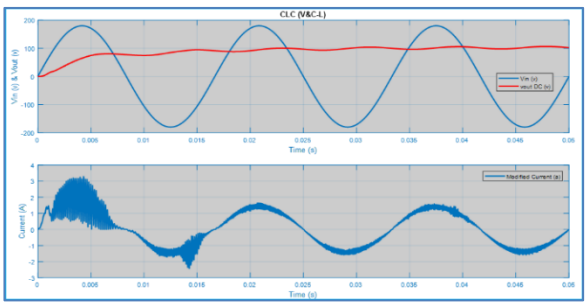


Fig. 14: Dynamic behavior for SEPIC-PFC for M-TLC (Voltage & Current –Loop) Control.

The Simulink results of the SEPIC-PFC before and after applying the control unit are shown in table 1.

Table 1: Simulink results of SEPIC-PFC

No	strategy	$THDi$ %	PF	DC-output Voltage
1	Without control	142.5	0.9455	1.772e-8
2	M-TLC (V-Loop)	7.398	0.9999	101.7
3	M-TLC (V&C-Loop)	5.484	1	100.3

Conclusion

In this paper, modified traditional linear control (M-TLC) is developed for SEPIC-PFC by applying an optimization algorithm and modified loop control. The SEPIC converter has been modeled by the CIECA method It is confirmed that SEPIC has a successful analysis, design, and modeling. It is an active technique, which has been operated as a step-up voltage regulator for automatic power factor correction. With unity power factor, 15% of THD reduction with unity power factor and regulated DC output voltage has been achieved. Thus, has been obtained better results compared to [20]. Simulink model shows that the steady-state is reached in a shorter time. The improved TLC controller technique can be implemented in various industrial applications because of its simplicity, low cost, and accuracy in its performance.

Appendix A. The numerical values of the structural parameters and operating conditions had given in Table 2 below.

Table 2: Design parameters of SEPIC and Control system specifications.

No	Parameters	Value	Unity
1	Mains voltage RMS-value($\mathbf{V_s}$)	127	v
2	Rated load power ($\mathbf{P_o}$)	100	W
3	Voltage reference ($\mathbf{V_{ref}}$)	5	v
4	Mains frequency ($\mathbf{f_o}$)	60	Hz
5	Carrier peak value. (VM)	1	v
6	Voltage sensor gain (H)	0.05	-
7	Proportional gain ($\mathbf{K_p}$)	0.22 & 0.05	-
8	Integral gain ($\mathbf{K_i}$)	9.7 & 25	-
9	Scalar ($\mathbf{K_v}$)gain	1/180	-
10	Scalar ($\mathbf{K_i}$)gain	5	-
11	Switching frequency (fs)	40k	Hz
12	$\mathbf{L_1}$ DC inductors	4m	H
13	$\mathbf{L_2}$ DC inductors	100µ	H
14	$\mathbf{C_1}$ DC capacitors	490n	F
15	$\mathbf{C_2}$ DC capacitors	330µ	F

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