International Journal of Current Engineering and Technology
E-ISSN 2277 – 4106, P-ISSN 2347 – 5161

Available at http://inpressco.com/category/ijcet

Research Article

Reconfigurable Hardware Implementation of Fused Add-Multiply Operator

Mohammed Ilyas Shaikh* **and Vishnu Suryawanshi**

G.H.R.I.E.T Wagholi, Pune, India

Accepted 20 June 2017, Available online 28 June 2017, **Vol.7, No.3 (June 2017)**

Abstract

Arithmetic operations are now a days used in digital signal processing applications. Here we will focused on implementation of fused add multiply operator. For getting recoding of sum of two numbers we will implement a technique called sum of two numbers in its modified booth. We introduce three different types of recoding technique. For using actual recoding technique we will compare with Fused add multiply designs. Here the technique which will be used that reduced some factors like delay, complexity of hardware and power consume of the Fused add multiply unit.

Keywords: *A-M operation, Different arithmetic circuit, Modified Booth recoding techniques.*

1. Introduction

In modern consumer electronics devices, Digital signal processing system is used which is providing Different technique for the Different multimedia and communications applications. A complicated digital signal processing technology have perform the different arithmetic operations and there implementation is based on different computational kernels, which are many techniques Fast Fourier transform, Discrete cosine transform, Finite impulse response filter and signals convolution. Performance of digital signal processing system are effected when they are doing the many complicated operations and the design which are considered for arithmetic operations. The research which are carried out now a days in which the operations which are carried out by the digital signal processing technique are so complicated. That is sharing of data and different operations in all the techniques the addition and multiplications are most hard operations which may be done by Finite impulse response filters. The Multiply and multiply accumulator these two techniques are consider as a good techniques for implementing a digital signal processing systems if we compare these with existing ones because they use very less sources. There are many techniques have been explain for implementing the multiply accumulator for reducing delay and critical path.

*Corresponding author **Mohammed Ilyas Shaikh** is a M.E [VLSI & Embedded System] scholar

2. Conventional Model

As we seen there are many techniques and a technology has been introduced for implementing the most simple and sophisticated multiply Accumulators. Multiply accumulator increase the data path synthesis of digital signal processing systems. For doing large amount of arithmetic calculations There are many digital signal processing system which are based only on the Add multiply instead of multiply accumulator and the multiply add techniques.

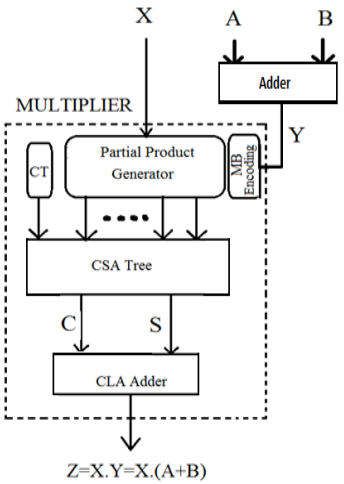

Fig 1 Existing Model

Add multiply technique is so simple in this technique we simply providing the adders output to the multipliers input which is considers as an so simple

technique and it is not applicable for many complicated arithmetic operatins.so it is better to avoid such simple techniques, will increases significantly area of the circuit and critical path delay of the circuit. It is actually increase the delay and critical path of the system, so it is an unacceptable technique for many complicated arithmetic operations. Now a days we require such a technique which takes less time and gives more output within respected time.

3. Proposed model and problem definition

In proposed technique we are increasing the flexibility of Add multiply operator which is as just simple technique, in this new model we are introducing the Fused technique actually which is depends on the sum of two numbers which comes in its modified booth. For sum of two numbers in its MB form needs to be implement a Fused add multiply operator as we compare it to its conventional form. This Fused add multiply technique done some of best work which are it reduced the delay means time taken by the operation will be as reduced as possible and power will consume less and again the complex hardware design will also be simple.

In fused add multiply technique with sum-modified booth recoding technique it is one of best technique Because it reduced the number of partial product and it also increase the calculation speed. It also decreases delay and reduces area and power which will be consumed. The technique which is sum to modified booth is an so simple technique which can be used for second compliment which we can say compliment of two and for unsigned numbers also. This can be comprised to odd and even bits. The new design of Add multiply operator is depend on fusion of adder and multiply encoding unit into a one data path. Block (Fig. 2) represent the direct recoding of the sum Y=A+B to its Modified booth design.

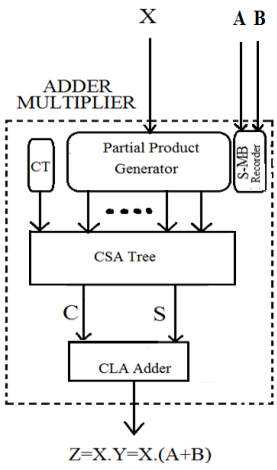

Fig 2 Proposed Model

The Above Diagram is fused technique which represents the direct recoding of the sum of and in its Modified Booth (MB) design. Here the multiplier which is used is an parallel multiplier to its modified booth form terms CT, carry save adder, and Carry look ahead adder these are used for the correction terms, the Carry-Save adder and last Carry look ahead Adder of the multipliers.

4. S-MB recoding technique

Conventional Signed HA's and FA's are used to design alternative schemes of the three S-MB recoding techniques. Each of the techniques can be applied in either signed and unsigned numbers which consist of odd or even number of bits. Consider that both the input A and B are in 2'nd complement form and it will consist of 2k bits in even case and 2k+1 in odd case to transform A and B(Y=A+B) in its modified booth representation those 3 SM-B scheme are,S-MB1,S-MB2 and S-MB3.

5. FAM Implementation

In multiplication the prevalent form i.e. booth algorithm (MB) is used. It is powerful algorithm in signed number multiplication. It works on both negative and positive number uniformly. In the FAM design presented in Fig.1 the multiplier is a parallel one based on the MB algorithm. Let us consider the product X.Y. The term Y=(Yn-1,Yn-2…Y1Y0)2's is encoded based on the MB algorithm and multiplied with X=(Xn-1,Xn-2...X1X2)2's.Both X and Y consist of n=2k bits and are in 2's complement from equation number below described the generation of the partial product.

Table 1: Modified Encoding Table

Binary				MB Encoding			Input carry
0	0	0	0	0	0	0	0
0	0	1	+1	0	1	0	0
0	1	0	+1	0	1	0	0
0	1	1	+2	0	0	1	0
1	0	0	-2	1	0	1	1
1	0	1	-1	1	1	0	1
1	1	0	-1	1	1	0	1
1	1	1	0	1	0	0	0

6. Performance Evaluation

6.1 Theoretical Analysis

In this section, we are analyzing and comparing the theoretical terms or factors. Here we are doing the observations based on three different techniques. Our observations will be on the basis of gate models. For our easy observation we will design on the basis on gates which are having only two inputs the gates are NAND, AND, NOR, OR .Here one gate will be equivalent of both area and critical delay. Area which will be taken by ha and fa equivalent to 3 and 7 gates. Sum of delay and carry which will be out is fa 4 and 3 gate. The whole design will be considered only on the full adder and the half adder.

6.2 Experimental Evaluations

Experimental Evaluations are depends on, comparisons of all the three techniques which will be used in the proposed technique. The programming which will be done for these techniques is a Verilog programming in vlsi Experimental observations are on the basis of sum to modified techniques. Comparison will be carried out here for getting all results.

6.2.1 Power Measurements

Below Table showing the comparative Measurements of power(Kostas Tsoumanis, 2014).

Table 2: Power Measurements

Power(mw)	
[1]	Project Result
37.20	34

Below Graphs show the different power measurements.

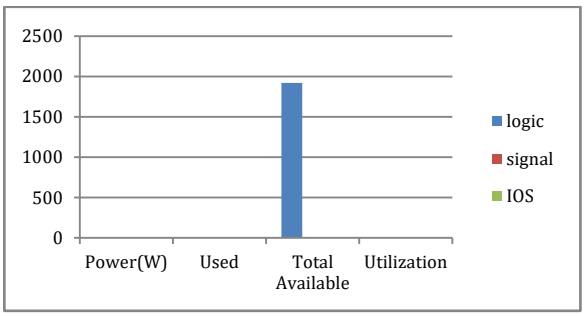

Fig 3 Power Measurement Graph for S-MB1

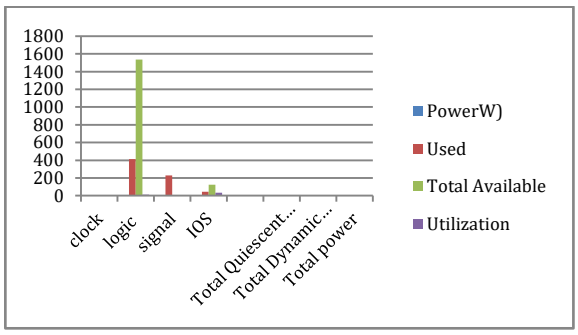

Fig 4 Power Measurement Graph for S-MB2

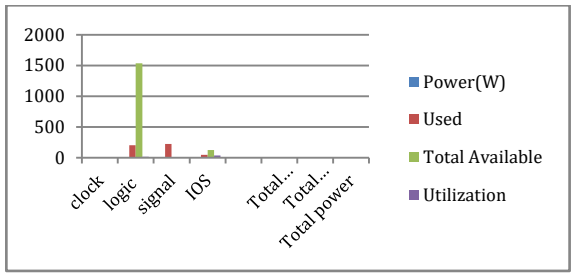

Fig 5 Power Measurement Graph for S-MB3

6.2.2 Delay Measurement

Below Table show the Delay Measurements (Sneha Vijayan, 2015).

Table 3 Delay Measurements

Delay(ns)	
[2]	Project Result
62.14	17.8

Below Graph Shows the Delay Measurement.

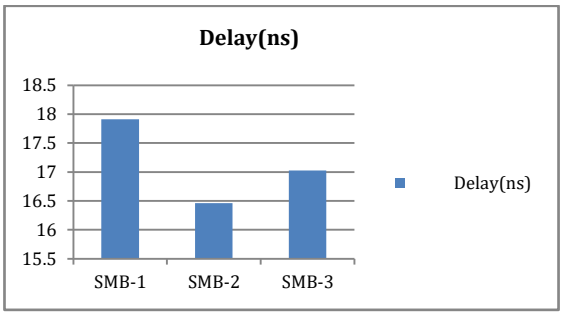

Fig 6.Graph for Delay Measurement

6.2.3 Area Measurement

Below table shows area Measurements (Sneha Vijayan, 2015).

Table 4: Area Measurements

Area		
	[2]	Project Result
Number of slice	374	8
Number of LUTs	770	117

Conclusion

Here we are comparing all the three techniques which are designed by using the newly suggested model. In this we are implementing the fused add multiply operator and then comparing all the techniques with the old technique which was depend on the only add multiply operator which was simple technique and taking more time for operations which are carried out by the existing technique. The technique which is used by us provides better results than previous which reduced the delay means taking less time, hardware design will simple.

Reference

Kostas Tsoumanis, Sotiris Xydis, Constantinos Efstathiou, Nikos Moschopoulos, and Kiamal Pekmestzi (April2014) Transactions on circuits and systems IEEE, vol.61,No.4,

Sneha Vijayan, Haripriya, (July 2015). Use of Compressors and Ladner Fischer Adder for the Design of Fused Sum Product Unit Using Advanced Booth Recoder Vol. 3, Issue 7,

M.Chitra Evangelin Christina (February 2015) An Efficient Design of Sum-Modified Booth Recoder for Fused Add-Multiply Operator (IJIET) Volume 5.

V.Karuppasamy, S.Muthukumar(April 2015). Design of Low Power Digital Low Pass FilterUsing FAM Vol.3, Special Issue 3.

B.Gopi Professor and HOD of ECE (April 2015) G.Kohila Implementation of FPGA based Hybrid Adder to Design Fused Add Multiply Operator using Modified Booth Recoder vol 5 issue 2.

A.Sindhu1, K.PriyaMeenakshi (November 2014) Implementation of Efficient Modified Booth Recoder for Fused Sum-Product Operator Vol. 2, Issue 11,.

Sneha Vijayan, Haripriya , (July 2015) Use of Compressors and Ladner Fischer Adder for the Design of Fused Sum Product Unit Using Advanced Booth Recoder Vol. 3, Issue 7.

P.R.Nivetha, R.Nihitha, P.Selvakumar (2015) Versatile Modified Booth Recoder Using SQRT CSLA Based S-MB Recoding TechniqueIJOER,Vol.3., Issue.3,.

M.Karthik, R.Prabhu (Mar 2015) Efficient Design Of Fixed Width Modified Post Truncated Booth Multiplier,IJREEE Volume 2 Issue 1.

S.Dhivya,Mr.T.Nallusamy(2015)RADIX-8 Modified Booth Recoder For High Speed ADD-Multiply Operator ,ICETSH ISSN: 2348 – 8549.

Shivaling S. Mahant-Shetti, Poras T. Balsara, (MARCH 1999).High Performance Low Power Array Multiplier Using Temporal Tiling, IEEE VOL. 7, NO. 1.

K. Ram Prakash(February 2014),Design and Implementation of Signed, Rounded and Truncated Multipliers using Modified Booth Algorithm for Dsp SystemsIJETAE, Volume 4, Special Issue 4.