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Research Article

Performance Evaluation of 8-Bit Vedic Multiplier with Brent Kung Adder

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Abstract

As multiplication influences the overall performance of system design, so the demand of high speed multipliers is increasing day by day. In this paper, 8X8 Vedic multiplier using Brent Kung adder is designed. Vedic Mathematics improves the speed of multiplier. It is the ancient Indian system of mathematics which is based on 16 sutras. Urdhva Tiryagbhyam sutra has been used for multiplication purpose. When design of Vedic multiplier using MUX based adder is compared with proposed multiplier, the proposed multiplier reduces delay .It is the advantage of proposed multiplier since it increases the speed. Verilog Hardware Description Language is used for coding. The proposed multipliers are synthesized using XILINX ISE 14.7. For simulation purpose ISim simulator has been used.

Keywords: *Brent Kung adder (BKA), Multiplier, Parallel Prefix Adder (PPA), Urdhva Tiryagbhyam, Vedic mathematics.*

1. Introduction

In most of the digital systems, multiplier and adder are the fundamental components in the design of application specific integrated circuits like RISC processors, digital signal processors (DSP), microprocessors etc. Now a day's high speed devices play key role in VLSI applications. So the designing of fast devices has become essential to fulfill the demand of end user. The overall performance of various systems depends upon adders and multipliers (Omanand, 2015).It is simple to perform binary multiplication than decimal multiplication (Subha, 2016). For multiplication operation performed in DSP applications, latency and throughput are the two major concerns from delay perspective. Latency is the real delay of computing a function, a measure of how long the inputs to a device are stable is the final result available on outputs. Throughput is the total number of multiplication which can be performed in given time (Sivaramakrishnan, 2013).

Over the past few decades, various architectures of multipliers have been designed. But Vedic multiplier is the fastest multiplier (Vucha, 2014).Among 16 sutras of Vedic mathematics; Urdhva Tiryagbhyam is a general formula which is applicable to all cases of multiplication. The speed of multiplier depends on type of adder. For high speed multiplication, fast adders are required. Parallel-prefix adders are known to have the best performance in VLSI designs. However, each type of parallel prefix adder has its own pros and cons and is chosen according to the design requirement of the application.

2. Related work

The comparison between array multiplier and Vedic multiplier w.r.t power, area and delay has been done this comparison is carried out to know the best architecture for multiplication. The results are compared for 8X8, 16X16 and 32X32 multipliers. It is found that Urdhva Tiryagbhyam multiplier is much more efficient compared to array multiplier and Nikhilam multiplier w.r.t delay and power. Vedic mathematics has many advantages (Harish, 2003).It is simple, regular and logical.

Comparison between Urdhva Tiryagbhyam and Nikhilam sutra based multipliers has been done in (Pande, 2012).The results show that Urdhva multiplier is faster for small inputs and Nikhilam multiplier is better for large inputs. This paper investigates novel architecture of Vedic multiplier which can easily select the appropriate Vedic multiplication sutra according to inputs.

This paper (Subha, 2016) proposed a high speed multiplier using Brent Kung (BK) CSLA. Quartus II Software has been used for synthesize the proposed architecture. Then RCA based CSLA and BEC based RCA CSLA multipliers are compared with BK based CSLA multiplier. The results show that proposed multiplier is faster than other two architectures. But the only

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disadvantage of this proposed multiplier is that the area is increased.

This paper (Vucha, 2014) describes another new architecture of Vedic multiplier which is the combination of Urdhva Tiryagbhyam sutra of Vedic maths for performing high speed multiplication and kogge stone algorithm for adding partial products. Kogge stone adder is a parallel prefix adder. The Verilog code of 8x8 proposed multiplier was synthesized using Xilinx ISE 9.1i. It is found that the proposed architecture reduces the delay. Paper (Sahani, 2013) presents the detailed study of Array multiplier, Constant coefficient multiplier and Urdhva Tiryagbhyam multiplier. The comparison result shows that Vedic multiplier is much faster.

In paper (Antony, 2015), a high speed multiplier is proposed using Urdhva Tiryagbhyam sutra and MUX based adder. The Experimental results shows that the proposed multiplier with mux based adder can achieve significant improvement in speed and area.

For high speed multiplication, Fast adders are in demand now days. Parallel prefix adder is faster than any other adders that have been created .PPA increases the speed of addition operation. Paper (Kipli, 2012) shows the comparison of Brent Kung adder and kogge stone adder. Results show that Brent Kung adder is efficient in terms of area, cost and delay, up to 16-bit. When bit size is more than 16 bit, kogge stone adder has very low delay compared to Brent Kung adder.

3. Objective

The prime goal of this work is to design and implement a fast 8 bit multiplier by combining the high speed feature of Urdhva Tiryagbhyam sutra and Brent Kung adder for minimizing the delay.

4. Vedic mathematics

The Vedic Mathematics is called so because of its origin from Vedas. It was rediscovered in early twentieth century by Jagadguru Swami Bharathi Krishna Tirthaji. This technique is based on 16 sutras and their 16 upa sutras (Charishma, 2012) .It can deal with all branches of mathematics like arithmetic, algebraic, trigonometry and geometry etc. It is fast, efficient and easy to learn and use (Adyanthaya, 2015). It reduces the complex calculations into simpler by applying 16 sutras.

Table 1: List of 16 Vedic sutras

S.No.	Name of Vedic Sutras	Meaning
1.	(Anurupye) Shunyamanyat	If one is in ratio, the otheris zero.
2.	Chalana Kalanabyham	Differences and similarities.
3.	Ekadhikina Purvena	One more than the previous one.
4.	Ekanyunena Purvena	The value is less than the previous one.
5.	Gunakasamuchyah	A factor of the sum is equal to the sum of factors.
6.	Gunitasamuchyah	The product of sum is equal to sum of the product.
7.	Nikhilam Navatashcaramam Dashatah	All from 9 and last from 10.
8.	Paraavartya Yojayet	Transpose and adjust.
9.	Puranapuranabyham	By the completion or non-completion
10.	Sankalana vyavakalanabhyam	By addition and by subtraction.
11.	Shunyams Saamyasamuccaye	When the sum is same then sum is zeros
12.	Sopaantyadvayamantyam	The ultimate and twice the penultimate.
13.	Shesanyankena Charamena	The remainders by the last digit
14.	Urdhva-Tiryagbhyam	Criss cross (Vertically and crosswise).
15.	Vyashtisamanstih	Part and Whole.
16.	Yaavadunam	Whatever the extent of its deficiency

4.1. Urdhva Tiryagbhyam

Urdhva Tiryagbhyam Sutra is a multiplication algorithm which is applicable to all cases of multiplication (Vucha, 2014).It simply means vertically and crosswise where the partial products are generated simultaneously which itself reduces delay and makes this method fast. This algorithm is applicable for the binary multiplication, so this Sutra has been chosen for implementation of Vedic multiplier.

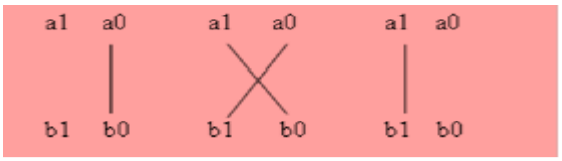

Fig 1: Line Diagram for 2x2 Bit binary multiplication using Urdhva Tiryagbhyam Sutra

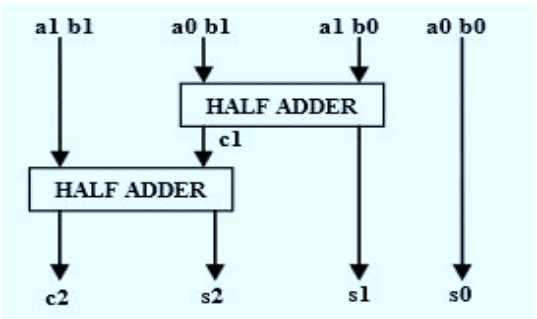

Fig 2: Block diagram of 2 X 2 Vedic Multiplier

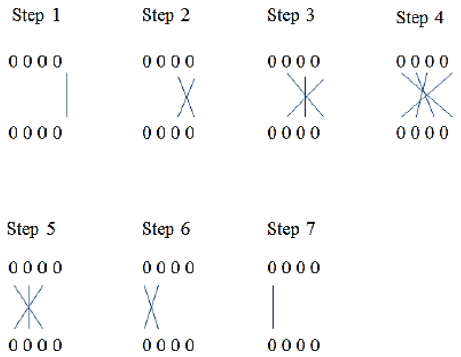

Fig 3: Line Diagram for 4X4 Bit binary multiplication using Urdhva Tiryagbhyam Sutra

A) *Algorithm for 4 X 4 Bit binary numbers Multiplication Using Urdhva Tiryagbhyam:*

A = A4A3 A1A0
X1 X0
B = B4B3 B1B0
Y1 Y0

X1 X0
* Y1 Y0

F E D C
CP = X0 * Y0 = C
CP = X1 * Y0 + X0 * Y1 = D
CP = X1 * Y1 = E
Where CP=Cross product

B) *Algorithm for 8 X 8 Bit binary numbers Multiplication Using Urdhva Tiryagbhyam:*

A = A7A6A5A4 A3A2A1A0
X1 X0
B = B7B6B5B4 B3B2B1B0
Y1 Y0

X1 X0
* Y1 Y0

F E D C

CP = X0 * Y0 = C
CP = X1 * Y0 + X0 * Y1 = D
CP = X1 * Y1 = E

Where CP=Cross product

5. Parallel prefix adder

The parallel prefix adder is one of the most popular architectures and offers good compromise among area, speed and power. It increases the speed of operations so these adders are widely used in high performance arithmetic systems in industries. The structure of parallel prefix addition is shown in Fig 4

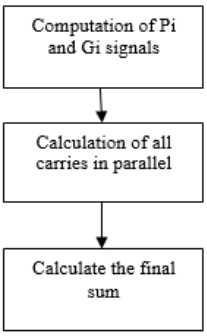

Fig 4: Addition procedure using Parallel Prefix tree structures

Parallel prefix addition is done in three simple steps:

a) Pre-processing stage

b) Carry generation network

c) Post processing stage

***A) Pre-processing stage*:** This step involves computation of generate and propagate signals corresponding to each pair of bits in A and B.

$P_i = A_i \text{ XOR } B_i$ (1)

$G_i = A_i . B_i$ (2)

B) *Carry generation network*: In this stage, carries corresponding to each bit are computed using the giving equation.

$Cp = Pi . Pj$ (3)

$Cg = Gi + Gj.Pi$ (4)

***C) Post processing stage*:** This is the final stage and it involves computation of sum bits. It is common for all adders and the sum bits are computed by logic equation 5 & 6:

$Si = Pi \text{ XOR } Ci - 1$ (5)

$Ci-1 = (Pi .Cin) + Gi$ (6)

5.1. Brent Kung adder

The Brent-Kung adder is one of the most advanced adder designs. Brent Kung adder is a parallel prefix form of carry- look ahead adder.

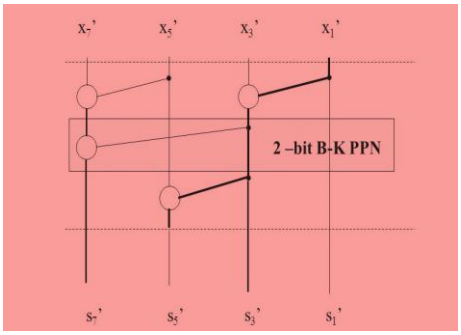

Fig 5: 4-bit Brent Kung adder

It was developed by Brent and Kung. PPA is the unique architecture of adders that uses generate and propagate signals. BKA takes less area than other PPAs.

Less cost and wiring congestion are other advantages of Brent Kung adder. It will increase the speed of partial product addition without compromising the power performance of the adder. It gives minimal number of calculating nodes but it has maximum logic depth and minimum area.

The parallel prefix graph of 4-bit and 8 –bit Brent-Kung adder is shown in figure 5 & 6 respectively.

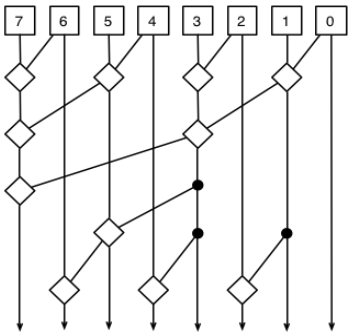

Fig 6: 8-bit Brent Kung adder

6. Design of the proposed 8-bit Vedic multiplier

In this section, the structure of designed Vedic multiplier is based on a unique technique of multiplication i.e. Urdhva Tiryagbhyam which is different from the traditional method of multiplication such as add and shift. For implementation of 8 x 8 multiplier, 2 x 2 Vedic multiplier is designed. Fig 2 shows block diagram of 2 X 2 bit Vedic multiplier. 2 x 2 Vedic multiplier is used as a basic building block for design of 4 x 4 bit Vedic multiplier. This is done by adding partial products using Brent Kung adders. Then by using 4 x 4 bit Vedic multiplier as a building block, 8 x 8 bit Vedic multiplier is designed as shown in Fig 7.

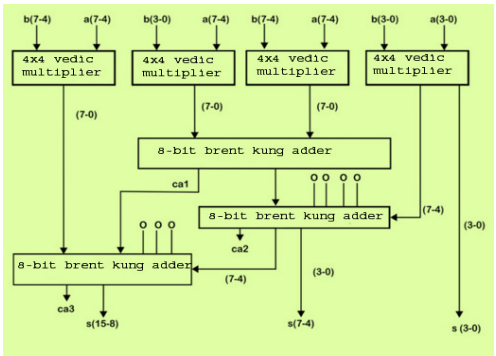

Fig 7: 8X8 Vedic multiplier using 8 bit Brent Kung adder

7. Results

7.1. Synthesis

Xilinx 14.7 has been used for synthesize the Verilog codes of multipliers. The RTL schematics of multiplier are generated and show in figure 8 & 9.

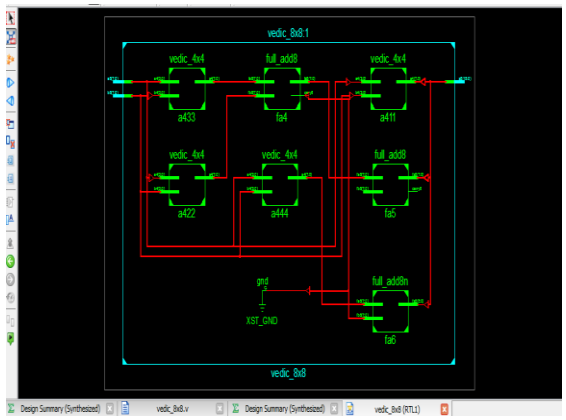

Fig 8: RTL view of 8-bit Vedic multiplier using MUX based adder

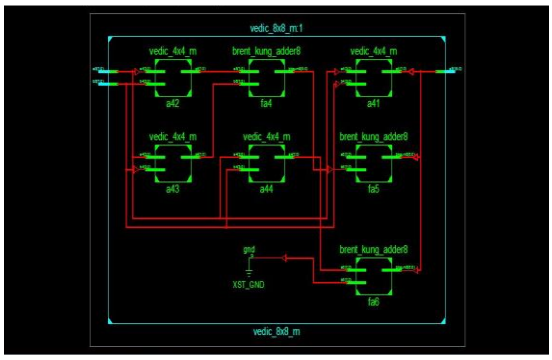

Fig 9: RTL view of 8 bit multiplier using Brent Kung Adder

7.2. Simulation

The functionality of each block is verified using simulation software i.e. ISim.

a) Simulation of 8-bit Vedic Multiplier using MUX based adder

The Simulation result for 8-bit Vedic multiplier using MUX based adder is shown in figure 10 in which a=11111111 and b=11111111 is taken and result c=1111111000000001 is obtained.

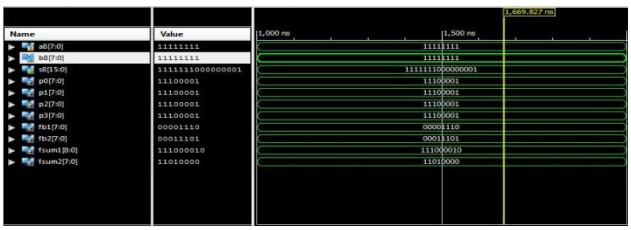

Fig 10: Simulation Result of 8-bit Vedic multiplier using Brent Kung adder

b) Simulation of proposed 8-bit Vedic Multiplier

The simulation result of proposed 8-bit Vedic multiplier for same set of inputs as used in Fig 10 is shown in Fig 11.

Fig 11: Simulation Result of 8-bit Vedic multiplier using MUX based adder

Table 2 shows the obtained results for 4 and 8 bit proposed Multipliers by combining Vedic Mathematics & Parallel prefix adder. The proposed Vedic multiplier is synthesized using Xilinx 14.7. Table 3 shows the results obtained by combining Vedic Mathematics & other technologies.

Table 2: Obtained results

Type	No. of Bits	No. of bonded IOs	Delay (ns)	No. Of Slices
Vedic multiplier using Brent Kung adder	4	16	3.165	31 out of 46560
	8	32	6.176	156 out of 46560

Table 3: Performance analysis

Multiplier	No. of bits	No. of bonded IOs	Delay (ns)
Vedic Multiplier using MUX based adder	8	32	8.894
Proposed Vedic Multiplier	8	32	6.176

Conclusions

Higher speed multipliers are required in many digital signal processing and image processing applications. In this paper, novel high speed architecture for multiplication by combining the features of Vedic multiplier & Brent Kung adder is proposed. As the number of bit increases from 4 x 4 bit to 8 x 8 bit, the timing delay greatly reduces for proposed Vedic multiplier as compared to Vedic multiplier using Mux Based multiplier. The results demonstrate that BKA based Vedic multiplier has delay of 6.13 ns and Vedic multiplier using MUX based full adder has delay of 8.89 ns.

Thus BKA based Vedic multiplier is found to have reduced delay by 30.6 %. The speed of BKA based multiplier is increased but the only limitation is that area is slightly increased. In Future, 16-bit and 32-bit BKA based multiplier can be implemented.

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