

Research Article

A Comparative Study of Static and Dynamic CMOS Logic

M.Roopa Nandini*, P.Mor and J.M. Keller

Department of Physics and Electronics, R.D.V.V., Jabalpur, India

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Abstract

The choice of the CMOS logic to be used for implementation of a given specification is usually dependent on the optimization and the performance constraints that the finished chip is required to meet. Several design options exist for CMOS combinational gates. One of the reliable, low-power design uses complementary static gates, where as high performance circuits uses dynamic logic styles which is more suitable for high speed. The performance of static logic is better than dynamic logic for designing basic logic gates like NAND and NOR however it is observed through studies that dynamic logic performance is better for higher fan in and complex logic circuits and also with the increasing level of integration, high performance, high speed and low power dissipation have become the mandatory requirements for any logic design. This paper presents a comparative study of CMOS static and dynamic logic.

Keywords: Static CMOS circuits, Dynamic CMOS circuits, Strong Zero, Strong One, Logic synthesis

Introduction

It is well known that, dynamic logic is less low-power consuming and have high speed than static logic (R.L.Geiger *et al* 2013). In particular, dynamic CMOS gates are supposed to be more advantageous than static ones mainly because of a total absence of output glitching and a reduced parasitic capacitance. However, the need of precharging operations introduces some extra power dissipation that does not affect static CMOS logic.

With the view to observe how the choice of the CMOS technology influences the behaviour, in terms of power consumption and delay of digital circuit, a study of CMOS static and Dynamic logic (P.S.Aswale *et al* 2013) has been presented. The study shows that power values of dynamic logic is lower than those for static logic and an appropriate choice of logic can lead to high performance, low power VLSI design.

Static and Dynamic Logic

Static logic

Static logic circuits allow versatile implementation of logic functions based on static, or steady-state, behaviour of simple CMOS structures or in other words commonly for combinational circuits (E.M.M.Poncino *et al* 1996) A typical static logic gate generates its output levels as long as the power supply is provided. This

approach, however, may require a large number of transistors to implement a function, and may cause considerable time delay.

Fig 1a shows the generalized block diagram of static logic (Jan.M.Rabaey *et al* 2002). It consists of a PULL UP network formed by P transistors and a PULL DOWN network formed by N transistors. Output rises to supply voltage V_{DD} when P network is ON and drops to Gnd when N network is ON. The basic function of static CMOS logic is explained with example of 2- input NAND gate as shown in 1b. There is conducting path between the output node and the ground only if input voltage V_A and V_B are equal to logic high value. If one of the inputs is at low logic value then there is a path created between supply voltage and output node. Thus except during switching, output connected to either V_{DD} or GND via a low resistance path.

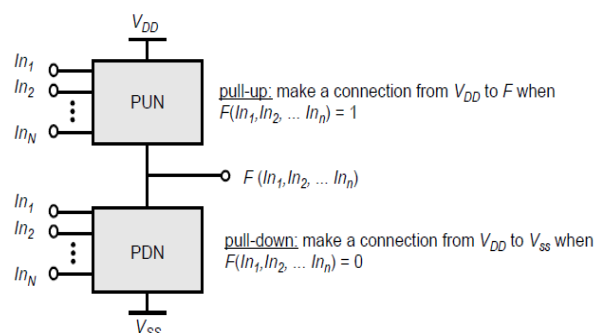


Fig 1a. Generalized Static Logic circuit

*The author **Roopa Nandini** is a Research Scholars, **Dr P Mor** is working as a Senior Scientific Officer, **Dr J.M. Keller** is working as a professor, at RDVV Jabalpur

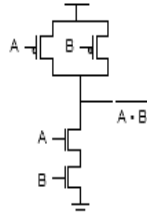


Fig 1b. NAND logic using Static CMOS

In constructing the PUN and PDN networks, the following observations should be kept in mind:

- A transistor can be thought of as a switch controlled by its gate signal. An nMOS switch is *on* when the controlling signal is high and is *off* when the controlling signal is low. A PMOS transistor acts as an inverse switch that is *on* when the controlling signal is low and *off* when the controlling signal is high.
- The PDN is constructed using nMOS devices, while pMOS transistors are used in the PUN. The primary reason for this choice is that nMOS transistors produce “strong zeros,” and pMOS devices generate “strong ones”.

To illustrate this, consider the examples shown in Figure 2 (Jan.M.Rabaey *et al* 2002). The output capacitance is initially charged to V_{DD} . Two possible discharge scenarios are shown in fig 2.a. An nMOS device pulls the output all the way down to GND, while a pMOS lowers the output no further than $|V_{Tp}|$ — the pMOS turns *off* at that point, and stops contributing discharge current. nMOS transistors are hence the preferred devices in the PDN. Similarly, two alternative approaches to charging up a capacitor are shown in Fig 2.b, with the output initially at GND. A pMOS switch succeeds in charging the output all the way to V_{DD} , while the nMOS device fails to raise the output above $V_{DD}-V_{Tn}$. This explains why pMOS transistors are preferentially used in a PUN.

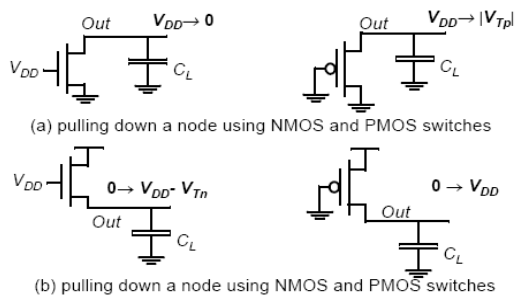


Fig 2. Simple examples illustrate why an nMOS should be used as a pull-down, and a pMOS should be used as a pull-up device.

Basic features of Static CMOS logic are (S.M.Kang *et al* 1999)

- Very low static power dissipation
- High noise margins (full rail to rail swing)
- Low output impedance, high input impedance
- No steady state path between VDD and GND

- Delay is function of load capacitance and transistor resistance
- Comparable rise and fall times (under the appropriate transistor sizing conditions).
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The speed of the static CMOS circuit depends on the transistor sizing and the various parasitics that are involved with it. The problem with this type of implementation is that for N fan-in gate $2N$ number of transistors are required, i.e., more area is required to implement logic. This has an impact on the capacitance and thus the speed of the gate.

Dynamic logic

In high density, high performance digital implementations where reduction of circuit delay and silicon area is a major objective, dynamic logic circuits offer several significant advantages over static logic circuits (S.M.Kang *et al* 1999; A.K.andy *et al* 2012). Dynamic circuit uses a clocked pull up transistor rather than a pMOS that is always ON (N.H.E.Weste *et al* 2005). Fig. 3a, shows a generalized CMOS dynamic logic circuit (Charles F.Hawkins *et al* 2004). The operation of all dynamic logic gates depends upon on temporary storage of charge in parasitic capacitance . (Jan.M.Rabaey *et al* 2002). This operational property necessitates periodic updating of internal node voltage levels, since stored charge in capacitor cannot retain indefinitely. Consequently, dynamic logic circuits require periodic clock signals in order to control charge refreshing. In the following, a dynamic CMOS circuit technique which allows us to significantly reduce the number of transistors used to implement any logic function is introduced. The circuit is based on first precharging the output node capacitance and subsequently, evaluating the output level according to the applied inputs.

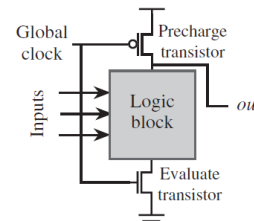


Fig. 3a. Generalized Dynamic Logic circuit

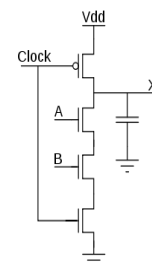


Fig 3b. 2 input NAND (Dynamic Logic)

Precharge

When $CLK = 0$, the output node *Out* is precharged to VDD by the pMOS transistor M_p . During this time, the evaluation nMOS transistor M_e is off, so that the pull-down path is disabled. The evaluation FET eliminates any static power that would be consumed during the precharge period (i.e., static current would flow between the supplies if both the pulldown and the precharge device were turned on simultaneously).

Evaluation

For $CLK = 1$, the precharge transistor M_p is off, and the evaluation transistor M_e is turned on. The output is conditionally discharged based on the input values and the pull-down topology. If the inputs are such that the PDN conducts, then a low resistance path exists between *Out* and GND and the output is discharged to GND . If the PDN is turned off, the precharged value remains stored on the output capacitance CL , which is a combination of junction capacitances, the wiring capacitance, and the input capacitance of the fan-out gates. During the evaluation phase, the only possible path between the output node and a supply rail is to GND . Consequently, once *Out* is discharged, it cannot be charged again till the next precharge operation. The inputs to the gate can, therefore make *at most one transition during evaluation*. Notice that the output can be in the *high-impedance state* during the evaluation period if the pull-down network is turned off. This behaviour is fundamentally different from the static counterpart that always has a low resistance path between the output and one of the power rails.

As an example, consider the circuit shown in Figure 3b. During the precharge phase ($CLK=0$), the output is precharged to VDD regardless of the input values since the evaluation device is turned off. During evaluation ($CLK=1$), a conducting path is created between *Out* and GND if (and only if) $A \cdot B$ is TRUE. Otherwise, the output remains at the precharged state of VDD . The following function is thus realized:

Basic features of Dynamic CMOS logic are (Jan.M.Rabaey *et al* 2002)

- Less number of transistors used to implement a logic results in optimizing area.
- Logic structure is ratioless.
- No static power dissipation.
- Less power consumption.
- Lower gate loading on logic signals results in high speed.
- Low output impedance, high input impedance.

Conclusions and Future Work

It has been observed from the study that the choice of static and dynamic CMOS logic depends upon the requirements of application. For simpler logic implementation, e.g. NAND, NOR etc., we can use static logic because they provide comparable performance with respect to dynamic logic at low cost and less complexity, whereas dynamic logic is preferable for complex logic circuit design like microprocessor, microcontroller (T.J.Thorp *et al* 2003). The present work is very useful for comparative study of analysis of static and dynamic CMOS circuits. An appropriate choice of logic along with voltage variation can lead to the design of high performance, low power VLSI chips.

This work shall be further carried out on bigger circuits like barrel shifter etc. so that we can analyze this comparative study more judiciously.

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