Research Article

Pipelined structure of Modified Booth's Multiplier

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Abstract

This paper describes a novel pipelined architecture of high speed modified Booth's multiplier. The proposed multiplier structure is based on modified Booth's algorithm and parallel processing techniques which are most widely used to accelerate the multiplication speed. The Carry and Save Adders are used for the intermediate stages and ripple carry adder for the last stage. Signed and unsigned multiplications can be done using the same hardware. Verilog HDL has been used to simulate the design and Xilinx has been used for delay measurement.

Keywords: Modified Booth's Algorithm, Parallel Processing, Pipelining

1. Introduction

Multipliers are key components of many high performance systems such as FIR filters,

Microprocessor, digital signal processors, etc.(Hsin-Lei Lin, 2004) and has various other applications. Multipliers are designed to achieve either of the following design targets – high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation.

The most common multiplication method is add and shift algorithm. The performance of the multiplier depends on the number of the partial products to be added. If the number of partial products is large, a large computation time is required. In add and shift design , the number of partial products generated are m*n, if the two numbers to be multiplied are of m and n bits. There are various multiplication algorithms such as Braun, Booth, modified Booth, Baugh-Wooley. Modified Booth algorithm is one of the most popular algorithms to reduce the number of partial products to be added. Wallace Tree algorithm can be used to reduce the number of sequential adding stages and hence high speed multiplier can be obtained. A high speed multiplier can be obtained by using both Modified Booth algorithm and Wallace Tree technique in one multiplier. However with increasing parallelism, the amount of shifts between the partial products and intermediate sums to be added will increase which may result in reduced speed, increase in silicon area due to irregularity of structure and also increased power consumption due to increase in interconnect resulting from complex routing.

2. Literature survey

It is possible to reduce the number of partial products by half (as compared to add and shift algorithm), by using the technique of radix 4 Booth recoding. The basic idea is that, instead of shifting and adding for every column of the multiplier term and multiplying by 1 or 0, we only take every second column, and multiply by ±1, ±2, or 0, to obtain the same results. Radix-4 booth encoder performs the process of encoding the multiplicand based on multiplier bits. Encoder and decoder circuit given below can be used to obtain partial product in the manner explained below.

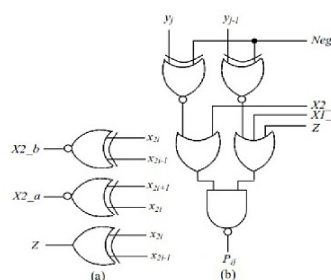| b_{i+1}	b_i	b_{i-1}	value	$X1\ a$	$X2\ b$	Z	Neg
0	0	0	0	1	0	1	0
0	0	1	1	0	1	1	0
0	1	0	1	0	1	0	0
0	1	1	2	1	0	0	0
1	0	0	-2	1	0	0	1
1	0	1	-1	0	1	0	1
1	1	0	-1	0	1	1	1
1	1	1	0	1	0	1	1

Fig.1 Encoder and Decoder Circuit used in Modified Booth's Algorithm

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The idea is to compare 3 bits at a time with overlapping technique. Grouping starts from the LSB, and the first block only uses two bits of the multiplier and assumes a zero for the third bit. The output of the encoder stage for all the possible combinations of three bits is given below in the table
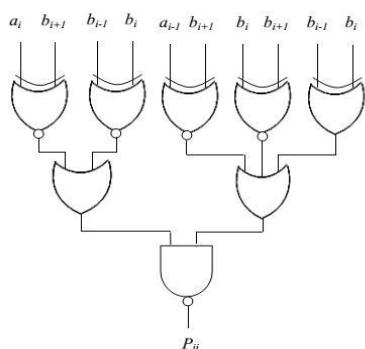

Fig.2 Combined circuit of encoder and decoder

The rows of partial products can be added using many techniques like Wallace tree. A simple full adder circuit which is used to add 3 bits to generate a sum and a carry bit can be implemented using 3:2 compressor circuit which have a better performance.

3. Proposed Work

Pipeline technique enhances the speed of a digital circuit to a great extent. In (N. R. Shanbag and P. Juneja,(Aug. 1988) Parallel implementation of a 44-bit multiplier using modified Booth"s algorithm, *IEEE J. Solid-State Circuits*, vol. 23, no. 4, pp. 1010–1013) modified Booth multiplier has been portioned into three pipelined stages. As most of delay is in the Wallace tree, performance can be improved by using carry save adders.

The algorithm described in this paper produces partial products with the help of modified booth's algorithm , using encoder and decoder given in (Soojin kim and Kyeongsoon Cho (2010),Design of High-Speed Modified Booth Multipliers Operating at GHz Ranges, *World Academy of Science, Engineering and Technology,* Issue 61, Jan. *2010)*. For 16*16 bits multiplication, a total of 9 rows of partial products have been generated using sign extension technique. Since carry propagation addition introduces significant delay ,3 rows of partial product have been taken at a time and using 32 full adders two rows of sum and carry each of 32 bits(with carry row shifted towards left by 1 bit) are generated. Similar procedure has been applied for the remaining two sets of rows. This leaves us with 3 sum rows and 3 carry rows with 1 bit shifted toward left for each carry row. Again 3 sum rows are added separately to generate 1 sum row and 1 bit shifted carry row. Similarly 1 sum and 1 carry row is generated for 3 carry rows. Out of the 4 generated rows , again 3 rows are taken and added in a similar fashion. Now, the generated two rows and one

previously generated remaining row are added to generate final sum and carry row. These two final rows are added using ripple carry adder with Cin=0 to generate final sum.The 32 full adders operate in parallel with no carries propagating between them. As a result, the delay introduced by multiple generation is minimized .

4. Experimental Results

On multiplying 1001110010110111*11111000101101010, we get the nine rows of partial products as A,B,C,A1,B1,C1,A12,B12,C12 as shown in the figure 4 below.
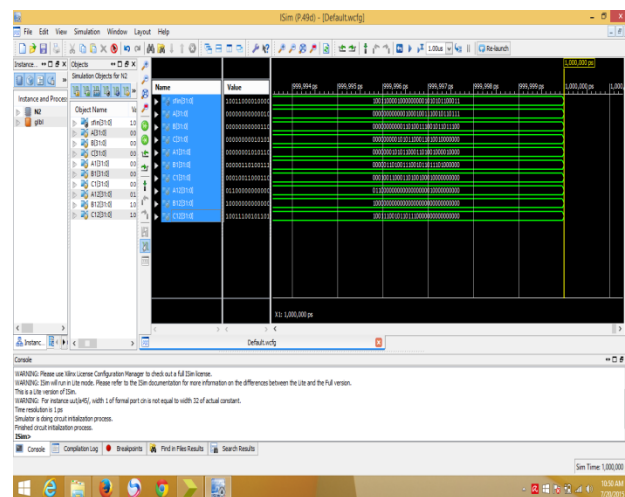
The final result is given by Sfin.

Fig.4 Simulation Result

Conclusions

Pipelined Multiplier based on Modified Booth Algorithm has been implemented for multiplication of two 16 bit numbers.

1) Number of logic levels=22.
2) Delay = 22.691ns.
3) Dynamic power dissipation =0 watts.
4) Slice Logic Utilization:
   Number of Slice LUTs : 380 out of 9112 4%
   Number used as logic : 380 out of 9112 4%

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