

Research Article

# Three Phase Seventeen Level Single Switch Cascaded Multilevel Inverter

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## Abstract

One of the major problems in electric power is power quality while converting from DC to AC is the harmonic contents. Multilevel inverters produce a staircase output voltage from DC voltage sources. Requiring great number of semiconductor switches and this is main disadvantage of the multilevel inverters. Application of multilevel inverter for high power equipments in industry has become popular because of its high-quality output waveform. In this paper, a three phase seventeen level single switch cascaded multilevel inverter is proposed with reduced number of switches, harmonic content and losses. An algorithm has been generated on the basis of optimized harmonic stepped wave form technique (OHSWT) to find out firing angle for multilevel inverter with unequal DC sources to reduce harmonic content present in output. The main attention behind the objective of proposed project seventeen level Single Switch Cascade multilevel inverter topology is to achieve the high power quality, low total harmonic distortion and better power factor. The harmonic content can be measured in terms of total harmonic distortion by using FFT analysis harmonic spectrum. The proposed multilevel inverter has been validated using MATLAB/SIMULINK software.

**Keywords:** Total harmonic distortion (THD), Optimized harmonic stepped waveform (OHSW), Cascaded H-bridge inverter (CHI), Voltage-source inverter (VSI), Multilevel inverters, Single Switch Cascade multilevel inverter (SSCMI), Fast Fourier analysis (FFT), insulated gate bipolar transistor (IGBT).

## 1. Introduction

Multilevel inverter includes an array of semiconductors and dc voltage sources, the output of which generate voltages with stepped waveforms (N Yousefpoor *et al*, 2009). In comparison with a two-level voltage-source inverter (VSI), the multilevel VSI enables to synthesize output voltages with reduced harmonic distortion and lower electromagnetic interference (Ebrahim Babaei *et al*, 2008). By increasing the number of levels in the multilevel inverters, the output voltages have more steps in generating a staircase waveform, which has a reduced harmonic distortion (E. Babaei *et al*, 2007). However, a larger number of levels increase the number of devices that must be controlled and the control complexity. Many industrial applications (J. Ebrahimi *et al*, 2011) have begun to use high power apparatus in recent year. Medium power motor drives and utilities require medium voltage and higher power level. In a medium voltage grid, connecting only one power semiconductor switch directly will create problem. To overcome this problem, a multilevel inverter topology

has been introduced as an alternative in medium voltage and high power situations. A multilevel inverter use renewable energy as source and can achieve high power rating. So, renewable energy sources such as solar, fuel cells and wind can be easily interfaced to a multilevel inverter structure for a high power application (Morteza Farsadi *et al*, 2013). The multilevel inverter concept has been used since past three decades (M. Malinowski *et al*, 2010). The multilevel inverter begins with a three-level inverter.

Thereafter, many multilevel inverter topologies have been developed. However, the main concept of a multilevel inverter is to achieve high power with use of many power semiconductor switches and numerous low voltage dc sources to obtain the power conversion that looklike a staircase voltage waveform. The dc voltage sources for multilevel (M. Farhadi Kangarlu *et al*, 2013), inverter are given by battery, renewable energy and capacitor voltage sources. The proper switching of the power switches combines these multiple dc sources to achieve high power output voltage. The voltage rating of the power semiconductor devices depends only upon the total peak value of the dc voltage source that is connected to the device. Three major classification of multilevel inverter structures

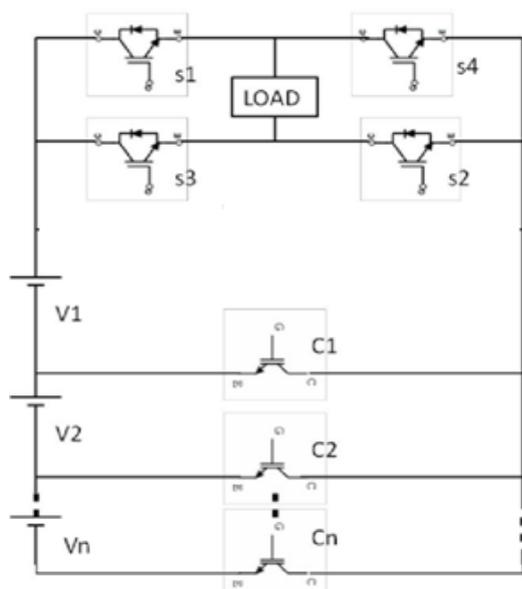
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are cascaded H-bridge inverter with separate dc source, diode clamped (neutral-clamped), and flying capacitor (capacitor clamped).

**2. The Proposed Project Three Phase Seventeen Level Single Switch Cascaded Multilevel Inverter**

*A. Single Switch Cascaded H Bridge Multilevel Inverter*

A new Single Switch Cascade multilevel inverter (SSCMI) has proposed and illustrated in Figure 2.1. The Single switch cascaded multilevel inverter (SSCMLI) consists of an H bridge inverter that is used to change the direction of current through the load to obtain an alternating current flow across the load. It consists of parallel connection of switches connected parallel to H bridge inverter with a unequal DC voltage source in between them.



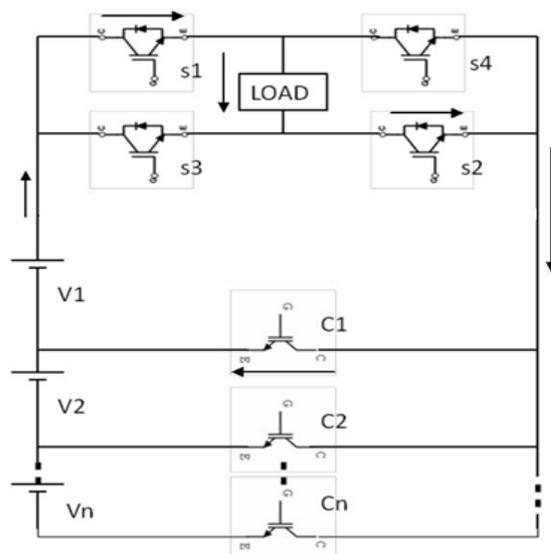
**Fig 2.1** Single switch cascaded H- Bridge multilevel inverter

Initially, switch s1 and s2 are turned on for supplying power in the positive direction across load. After positive cycle is finished switches s1 and s2 are turned off. Now for reversing the direction of flow of power across load, switches s3 and s4 are turned on. At the end of negative cycle, switches s3 and s4 are turned off. There is a period of gap is left between positive to negative cycle and negative to positive cycle, in that period switch R is turned on and turned off for continuous conduction of current across the load that is stored in the load if its inductive and this switch is useful in reducing voltage ripple that occur in between cycles due to inductive loads.

In positive cycle operation, after the switches s1 and s2 are turned on, load is across the voltage sources and the amount of voltage to be present across it is decided by the switches C1, C2.....Cn. Switch c1 is turned on along with s1 and s2 to apply a voltage of E across load in positive direction which is showed in the

Figure 2.2. Now, switch c1 is turned off and c2 is turned on to apply a voltage of 2E across the load. This operation is repeated until peak voltage nE is obtained; where n represent number of dc voltage source. Then switch Cn is turned off and cn-1 is turned on to reduce the voltage level from peak to low to form a positive cycle.

In negative cycle operation, switches s3 and s4 are turned on, then load is connected across the voltage sources and the amount of voltage to be present across it is decided by the switches C1, C2.....Cn. Switch c1 is turned on along with s3 and s4 to apply a voltage of E across load in negative direction which is showed in the Figure 2.3.



**Fig 2.2** Positive cycle operation

This process is repeated until the peak negative  $-nE$  is reached and then switch Cn is turned off. Switches turned on in the reverse direction from Cn to C1 to apply a voltage of nE to E in decreased way to form a complete negative cycle.

The unidirectional switches consist of an insulated gate bipolar transistor (IGBT) with an anti parallel diode. The switches S1, S1, S (n+2)/2, and S (n+2)/2 are unidirectional and the other switches are bidirectional; hence, they have to withstand both positive and negative voltages. For instance, when S(n+2)/2 is turned ON, the voltage Vdc is on the switch Sn /2 , and if the switch S(n-2)/2 is turned ON, the voltage equal to -Vdc is on the switch Sn /2 . The same conditions are valid for the other switches. Therefore, the switches have to withstand both positive and negative voltages. In addition, the switches have to conduct backward current that is as a result of inductive characteristic of the load. It can be concluded that the switches must be bidirectional. There are several circuit configurations for bidirectional switches. In this study, the common emitter topology is used as it needs one gate driver for a switch. Considering the types of the switches, 2n IGBTs are required in the proposed sub multilevel inverter.

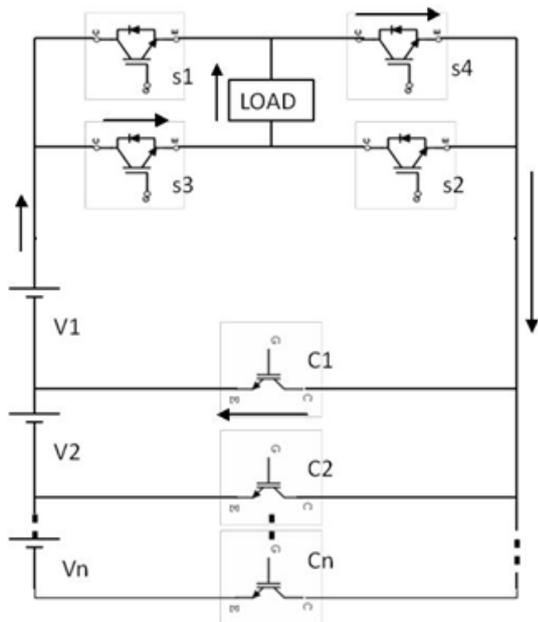


Fig 2.3 Negative cycle operation

B. Cascaded H-Bridge Multi-Level Inverter Structure: A cascaded multi-level inverter consists of a number of H-bridge (single-phase full-bridge) inverter units. The general function of this multi-level inverter is to synthesize a desired voltage from several separate dc sources (SDCSs), which may be obtained from solar cells, fuel cells, batteries, ultra-capacitors, etc. Fig. 1 shows a single-phase structure of a cascade multi-inverter with five SDCSs. Each dc source is connected to a single-phase full-bridge inverter. Each inverter can generate three different output voltages,  $+V_i$ , 0 and  $-V_i$  according to the states of the four switching devices. The ac output of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of all individual inverter outputs. The number of output voltage levels in a cascaded multi-level inverter is then  $2S+1$ , where  $S$  is the number of dc sources. An example phase voltage waveform for an seventeen-level cascaded multi-level inverter with five SDCSs ( $S=8$ ) and five full bridges is shown in Figure 2.1 The output voltage is given by  $V_{an}=V_1+V_2+V_3+V_4+V_5+V_6+V_7+V_8$ . With a large of levels and an appropriate switching algorithm, the multi-level inverter results in an output voltage that is almost sinusoidal.

Table 1 Voltage Values And On State Switches For Seventeen Level Proposed Topology

level	Switches in on state	Voltage
8	s1,s2	C8
7		C7
6		C6
5		C5
4		C4
3		C3
2		C2
1		C1

0			0
-1	s3,s4	C1	V1
-2		C2	V2+V1
-3		C3	V3+V2+V1
-4		C4	V4+V3+V2+V1
-5			V5+V4+V3+V2+V1
-6		C6	V6+V5+V4+V3+V2+V1
-7		C7	V7+V6+V5+V4+V3+V2+V1
-8		C8	V8+V7+V6+V5+V4+V3+V2+V1

### 3. Optimized Harmonic Stepped wave form Technique

The objective here is to determine the switching angles  $0^\circ < \theta_1 < \theta_2 < \dots < \theta_s < 90^\circ$  so as to eliminate (S-1) certain lower frequency harmonics from the output voltage waveform while generating the desired fundamental component,  $V_f$ . This necessitates, mathematically, solving  $S$  equations derived from equation (1). The mathematical statement of these conditions is as follows:

$$[V_1 \cos(\theta_1)+V_2 \cos(\theta_2) + \dots + V_s \cos(\theta_s)] = m_a$$

$$[V_1 \cos(3\theta_1)+V_2 \cos(3\theta_2)+\dots + V_s \cos(3\theta_s)] = 0$$

$$[V_1 \cos(5\theta_1) + V_2 \cos(5\theta_2) + \dots + V_s \cos(5\theta_s)] = 0$$

$$[V_1 \cos(h\theta_1)+V_2 \cos(h\theta_2)+\dots + V_s \cos(h\theta_s)] = 0$$

In which  $h$  is the highest order of the harmonics to be eliminated, Note that for three-phase, three-wire systems, and the triplen harmonics in each phase need not to be eliminated, as they are automatically cancelled in the line- to-line voltage.

Assuming  $V_{dc}=V_1+V_2+\dots+V_s$ ,  $m_a=V_f / (4.V_{dc}/\pi)$

$$V_{1dc}=V_1/V_{dc}, V_{2dc}=V_2/V_{dc} \dots$$

$V_{Sdc}=V_s/V_{dc}$ , equations (1) can be rewritten as:

$$[V_{1dc} \cos(\theta_1)+V_{2dc} \cos(\theta_2) + \dots + V_{Sdc} \cos(\theta_s)] = m_a$$

$$[V_{1dc} \cos(3\theta_1)+ V_{2dc} \cos(3\theta_2)+\dots + V_{Sdc} \cos(3\theta_s)] = 0$$

$$[V_{1dc} \cos(5\theta_1) + V_{2dc} \cos(5\theta_2) + \dots + V_{Sdc} \cos(5\theta_s)] = 0$$

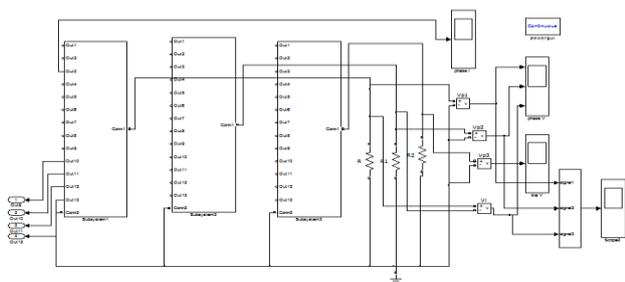
$$[V_{1dc} \cos(h\theta_1) + V_{2dc} \cos(h\theta_2) + \dots + V_{Sdc} \cos(h\theta_s)] = 0$$

Equations have been set up, from which, the switching angles  $\theta_1, \theta_2, \dots, \theta_n$  can be calculated. These equations are nonlinear as well as transcendental in nature, which suggests a possibility of multiple solutions. Usually, the Newton-Raphson method, mathematical Resultant theory, and Homotopy algorithm are used to solve such nonlinear equation systems. In this paper, Homotopy algorithm is used, which solves the transcendental equations with a much simpler formulation. The optimized harmonic stepped waveform (OHSW) technique was used in this paper.

When OHSW technique is employed along with the multilevel topology, THD of output waveform is reduced without using any filter circuit is possible. Switching devices are turn on and turn off only one time in a complete cycle. Thus, switching loss and EMI problem can be overcome. Fig. 4 shows a simulation circuit for proposed project three phase seventeen level single switch cascaded multi inverter simulation diagram.

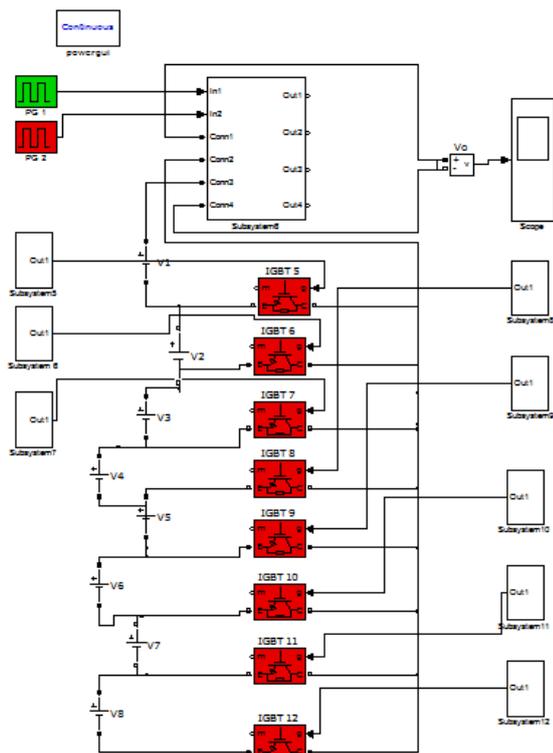
**4. Simulation Results**

*A. Three phase seventeen-level single switch cascaded multilevel inverter is shown in figure 4.1*

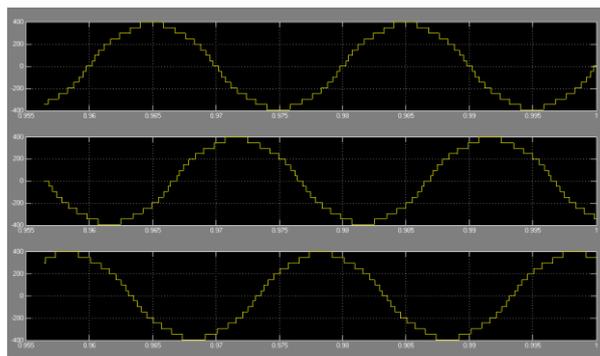


**Fig 4.1** Simulation circuit for proposed project three phase seventeen level single switch cascaded multilevel inverter

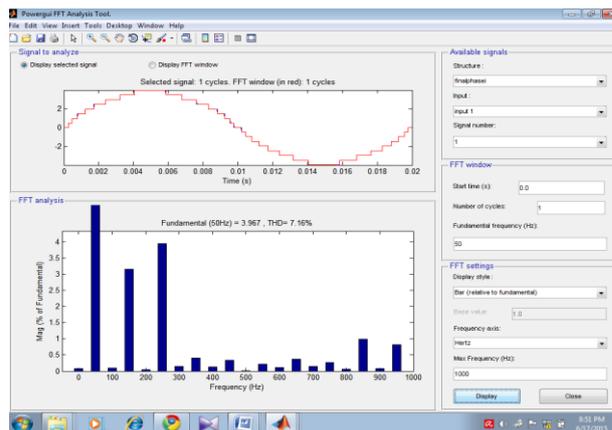
*B. Single phase seventeen-level single switch cascaded multilevel inverter is shown in figure 4.2*



**Fig 4.2** Simulation circuit for proposed project single phase seventeen level single switch cascaded multilevel inverter

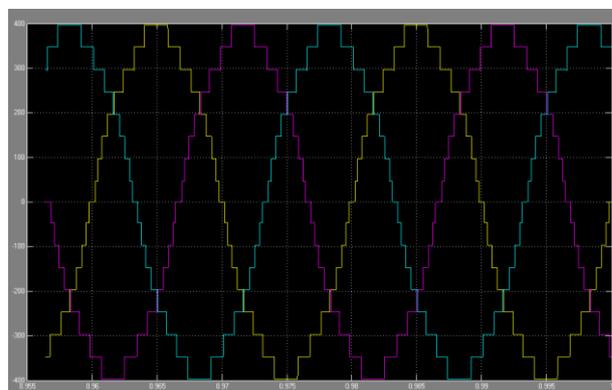


**Fig 4.3** Output voltage wave forms for the single phase seventeen level SSCMI



**Fig 4.4** THD (Total Harmonic Distortion) current for the proposed three phase seventeen level SSCMI

The output voltage waveform for Single switch cascaded multilevel inverter as shown in figure 4.3 and FFT Analysis on output current waveform is shown in the figure 4.4 and Total Harmonic Distortion in MATLAB is 7.16%.



**Fig 4.5** Output Voltage waveform of Three Phase Single switch cascaded multilevel inverter in MATLAB

**Conclusion**

The need for efficient power conversion due to the explosive growth in renewable energy and reduced output ripple for sensitive devices has increased the

demand for multilevel inverter. Multilevel inverters are very interesting for high voltage applications, energy conversion and considerably improve the output voltage quality. This paper has proposed a new topology of the cascaded converter called Cascaded Sub-Multilevel Cells. The main advantages of the Single Switch Cascade multilevel inverter (SSCMI) are:

- Improve the output voltage quality
- Reduced number of switching devices, cost & complexity
- Improves the power factor
- Small on-state voltage drop and conduction losses
- Reduction of  $dv/dt$  stresses on the load

Using optimized harmonic stepped waveform technique. The output waveform of Three Phase Single switch cascaded multilevel inverter circuit was simulated using MATLAB. The total harmonic content present in the output current of proposed circuit after applying OHSW is 7.16% in MATLAB.

## References

- Malinowski, M. Gopakumar, K. Rodriguez, J. and Perez, M. (2010), *A Survey On Cascaded Multilevel Inverter*, IEEE transaction on Industrial Electronics, volume 57, no. 7, pp. 2197-2206.
- Farhadi Kangarlu, M. Babaei, E. (2013), *A generalized cascaded multilevel inverter using series connection of submultilevel inverter*, IEEE Transaction on Power Electronics, volume 28, no. 2, pp. 625-636.
- Ebrahimi, J. Babaei, E. and Gharehpetian, G.B. (2011), *A new topology of cascaded multilevel converters with reduced number of components for high-voltage applications*, IEEE Transaction on Power Electronics, volume 26, no. 11, pp. 3119-3130
- Ebrahim Babaei (2008), *A cascade multilevel converter topology with reduced number of switches*, IEEE Transaction on Power Electronics, volume 23, no. 6, pp. 2657-2664
- Manjrekar, M. Lipo, T.A. (1998), *A hybrid multilevel inverter topology for drive application*, Proceedings of APEC, pp. 523-529.
- Babaei, E. Hosseini, S.H. Gharehpetian, G.B. Tarafdar Haque, M. and Sabahi, M. (2007), *Reduction of dc voltage sources and switches in asymmetrical multilevel converters using a novel topology*, Electric Power System Research, volume 77, no. 8, pp. 1073-1085.
- Babaei E. and Moeinian, M. S.(2010), *Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem*, Energy Conversion and Management, volume 51, no. 11, pp. 2272-2278.
- Zahra Bayat (2012) and Ebrahim Babaei, *A New Cascaded Multilevel Inverter with Reduced Number of Switches*, IEEE conference on power electronics.
- Rufer, A. Veenstra, M. and Gopakumar, A. (1999), *Asymmetric multilevel converter for high resolution voltage phasor generation*, in Proc. Eur. Conf. Power Electron. Appl., Lausanne, Switzerland, pp. 1-10
- Morteza Farsadi, Vafamehr, A. and Farhadi Kangarlu, M.(2013), *Cascaded Multilevel Converter Using Five-Level Power Cells*, Aust. J. Basic & Appl. Sci., 7(4): 546-553.

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