

Research Article

Design and Implementation of Huffman Decoder for Text data Compression

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Abstract

Digital compression of data is important due to the bandwidth limitations inherent in the transmission medium. Data compression is also called as source coding. It is the process of encoding information using fewer bits than an uncoded representation. Compression is a technology for reducing the quantity of data used to represent any content without excessively reducing the quality of the picture. It also reduces the number of bits required to store and/or transmit digital media. Compression is a technique that makes storing easier for large amount of data. There are various techniques available for compression, this paper presents Huffman decoder based on new binary tree method for improving usage of memory and Bandwidth for Text data Compression. The work mainly deals with the implementation of Huffman decoder on a Xilinx 14.7 version, using Verilog Hardware Description Language.

Keywords: Binary tree, Data compression, Decoding algorithm Huffman decoder, Verilog, FPGA.

1. Introduction

Compression is a necessity in the current world of technology, which is centered on speed and efficiency. Consequently, large and bulky pieces of information are abandoned for smaller bits of data, which can be shared between peers at faster rates. Data can be broken into smaller pieces or forcefully compressed by programs that are powered by algorithms. The two major types of compression algorithms are lossless compression and lossy compression. Lossless compression is used for applications that require an exact reconstruction of the original data, while lossy compression is used when the user can tolerate some differences between the original and reconstructed representations of the data. Lossy compression techniques involve some loss of information and data are compressed using lossy techniques generally cannot be recovered or reconstructed exactly. In return for accepting this distortion in the reconstruction, we can generally obtain much higher compression ratios than is possible with lossless compression. An important element in the design of data compression algorithms is the modeling of the data. The extremely fast growth of data that needs to be stored and transferred has given rise to the demands of better transmission and storage techniques. Various lossless data compression algorithms have been proposed and used. Huffman Coding, Arithmetic Coding, Shannon Fano Algorithm, Run Length Encoding Algorithm are some of the techniques in use. David Huffman as part of

a class assignment developed the Huffman coding algorithm. Huffman codes are prefix codes and are optimum for a set of probabilities. The Huffman code is based on two observations. First, in an optimum code, symbols that occur more frequently (have a higher probability of occurrence) have shorter codewords than symbols that occur less frequently. Second, in an optimum code, the two symbols that occur least frequently have the same length. The Huffman procedure is obtained by adding a simple requirement to these two observations. This requirement is that the codewords corresponding to the two lowest probability symbols differ only in the last bit.

2. Preliminary

A Huffman decoder is implemented for text. The text compression involves its encoding; the text decoder contains the Huffman decoder for obtaining the original text.

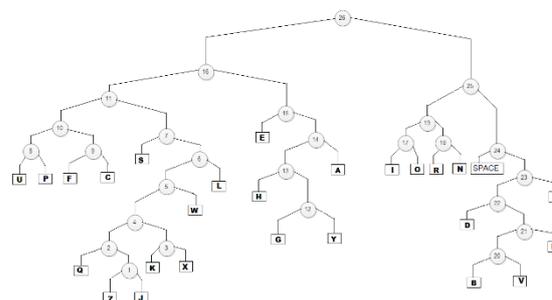


Fig 2.1 Binary trees for Text

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The Huffman tree used by encoder and decoder is shown in Fig2.1. The alphabet consists of the uppercase letters and the space. All left branches are labeled 0, and all right branches are labeled 1. This tree is based on the following assumed frequencies E 130 T 93 N 78 R 77 I 74 O 74 A 73 S 63 D 44 H 35 L 35 C 30 F 28 P 27 U 27 M 25 Y 19 G 16 W 16 V 13 B 9 X 5 K 3 Q 3 J 2 Z 1

It is assumed that there are 130 Es and 182 spaces for every 1000 letters. The encoder retrieves the code for each symbol from a map, and shifts it out one bit at the time. The decoder is a finite state machine whose state transition graph is obtained from the tree by adding acs from the leaves back to the top of the tree. Each node uses ten bits for its encoding. The code of the root is 0. If a state is not a leaf of the tree, and its encoding is n, then the encodings of its two children are 2n+1 and 2n+2.

2.1 Implementation of Huffman Encoder

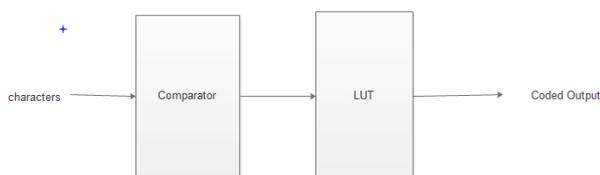


Fig.2.2 Block diagram of Encoder

The Fig.2.2 shows the block diagram of encoder and code for each character which comes from the tree stored in the LUT. Character input which is given to the encoder is stored inside the LUT. Therefore, the output of the encoder block will be these stored values inside the LUT.

2.1 Implementation of Huffman decoder

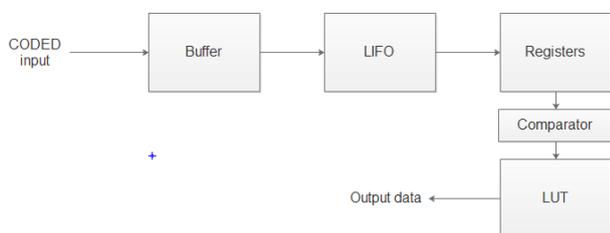


Fig.2.3 Block diagram of Decoder

The fig 2.3 shows the block diagram for the decoder in which the coded value is first stored in the buffer then it is shifted using a LIFO, The shifted value is then stored in the 9 bit temporary register which is then compared with respective codes stored in the LUT and finally the character is decoded.

3. The Proposed Method

In the Proposed method a Huffman tree is implemented using the binary tree which is built upon using the frequencies corresponding to the characters

shown in fig2.1 and Fig3.1. Figure 3.1 shows a binary tree in which the branch values are mentioned based on its construction using the characters and respective frequencies given.

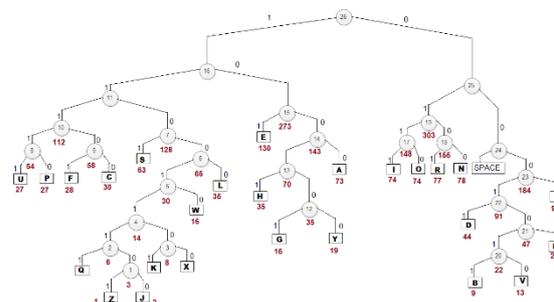


Fig 3.1 binary trees with corresponding codes for Text

3.1 Implementation of Proposed Huffman Encoder

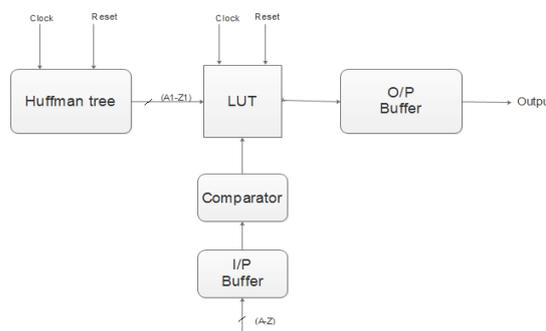


Fig.3.1 Block diagram of Proposed Encoder

In this proposed work the Encoder is implemented using a Huffman tree. A Huffman tree is implemented in Verilog platform using the binary tree shown in the fig 2.1. This preimplemented Huffman tree is stored in the LUT to give the corresponding encoded output in correspondence to the character.

3.2 Implementation of Proposed Huffman Decoder

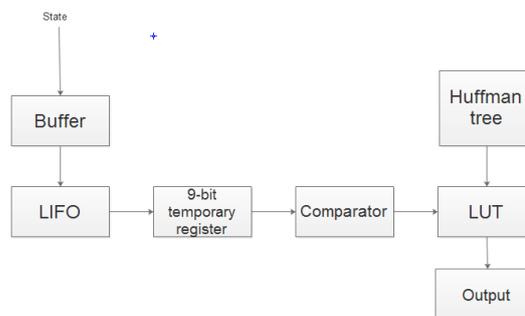


Fig.3.1 Block diagram of Proposed Decoder

Both the encoding and decoding should done with respect to the same tree. so that the data stored in the encoder block is stored in the encoder LUT is stored in the decoder LUT. In the proposed method, inside the

decoder block first a buffer is present in order to store the output of the encoder part. A LIFO is present next to it which will shift the coded values stored inside the Buffer. This shifted code is then stored inside a temporary register of 9-bit size. Both this coded value and the predetermined Huffman tree which is stored inside the LUT is compared to obtain a decoded output with respect to the corresponding coded state.

4. Simulation Results for Text using the Proposed Method

A Huffman Encoder and decoder is designed, described in Verilog and implemented on a Xilinx Virtex 5 FPGA using ISE 14.7. The design aims to achieve high operating frequencies using few logical resources. The functional simulation for the Huffman encoder and decoder block is carried out using the ISE design suite 14.7

The binary tree for the characters based on the assumed frequencies E 130 T 93 N 78 R 77 I 74 O 74 A 73 S 63 D 44 H 35 L 35 C 30 F 28 P 27 U 27 M 25 Y 19 G 16 W 16 V 13 B 9 X 5 K 3 Q 3 J 2 Z 1 is shown below.

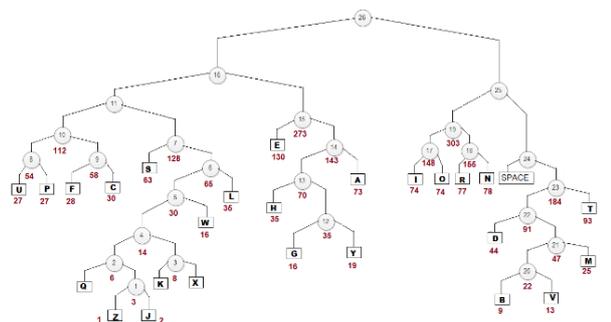


Fig.4.1 Binary tree based on the assumed frequencies

The Simulation results for the tree is obtained .In this the data value corresponding to the branch is shown in fig4.2.

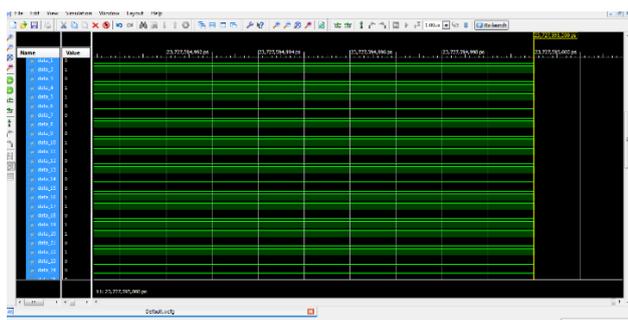


Fig.4.2 Branch value corresponding to the tree

The binary values for the frequencies corresponding to the characters is shown in fig4.3

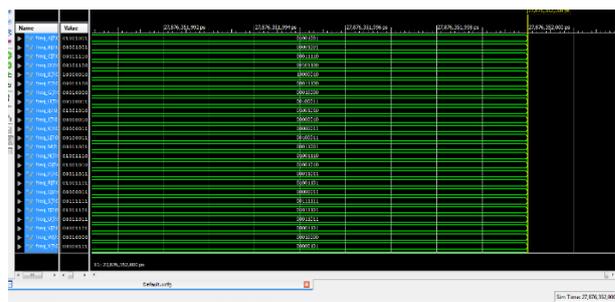


Fig.4.3 Simulated output of the Branch value corresponding to the tree

Fig 4.4 shows the node values of the tree corresponding binary formed on the basis of the assumed frequencies.

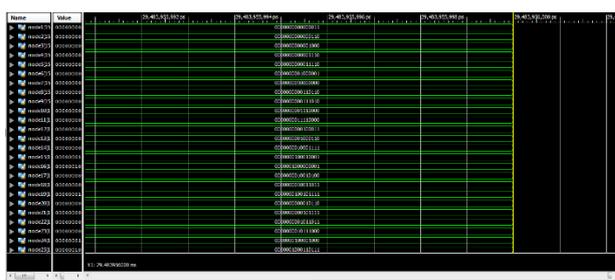


Fig.4.3 Simulated output of the branch values of the binary tree

The simulated result of the Encoder for output of a word is obtained using the Xilinx 14.7

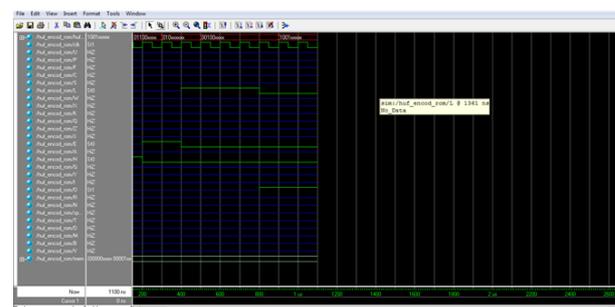


Fig.4.4 Simulated output of the word HELLO

The output of the encoder is given as the input to the buffer in the decoder block the value is compared with the LUT and the decoded output is obtained



Fig.4.5 Simulated decoded output of the word HELLO

In Fig 4.4, the input signal is a 5-bit input signal which acts as the address to the LUT in the encoder stage which gives corresponding alphabetical outputs. Encode is the serial output stream which given as input to the decoder. Is the decoded character output from the decoder. The encoding and decoding operations are performed for the text HELLO. The simulation results for HELLO text reveal that only 22 bits are required to store it whereas 40 bits are required for the original text. Hence original data can be retrieved easily and requires less memory by using the new binary tree algorithm method

Conclusion

This research will show that the higher data redundancy helps to achieve more compression. The presented new compression and decompression technique based on Huffman tree for scan testing is used to reduce test data size and test application time. At Present Started with designing a Huffman encoder and decoder in Verilog platform. Huffman decoder using Binary tree algorithm was implemented on Verilog and FPGA platforms. The Architecture implemented by VERILOG Design, using XIINX 14.7 version. Future works needs to be carried out to improve the area. On comparing with other different compression techniques, came to a conclusion that Huffman coding is efficient technique for image compression and decompression to some extent.

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