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Research Article

Clock Tree Synthesis based on Wire length Minimization Algorithm

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Abstract

Clock Distribution Network is to be designed carefully to optimize many performance criteria like power, area and delay. The reduced process size necessitates better distribution strategies and algorithms. In this paper, a hierarchical clock network design by making use of the diagonal routes is presented. Buffers are introduced to get perfect pulse width, duty cycle and latency.

Keywords: *Clock Tree Synthesis, Exact zero skew, Buffer insertion, delay minimization, Matlab, Spice*

1. Introduction

Clock signals are typically loaded with the greatest fan out, travel over the longest distances and span the entire chip, and operate at the highest speeds of any signal, either control or data, within the entire system. The clock signals are particularly affected by technology scaling, because long global interconnect lines become much more highly resistive as line dimensions are decreased. This increased line resistance is one of the primary reasons for the growing importance of clock distribution on synchronous performance. Finally, the control of any differences in the delay of the clock signals can severely limit the maximum performance of the entire system as well as create catastrophic race conditions in which an incorrect data signal may latch within a register (E. G. Friedman, 2001). The control of any differences in the delay of the clock signals can severely limit the maximum performance of the entire system as well as create catastrophic race conditions in which an incorrect data signal may latch within a register. With the careful design of the clock distribution network, system-level synchronous performance can actually increase (Wann and Franklin, 1982; Wann and Franklin, 1983).

Duty of the clock distribution network is to provide clock signal to each node/register in the synchronous digital circuit. So the circuit structure will influence clock distribution network structure or vice versa. There are many existing clock distribution techniques, each focusing in various areas of optimizations.

There have been many researches on routing algorithms to minimize clock skew. Exact zero skew has been achieved by structures like H-tree (F. Anceau, 1982; H.P. Bakoglu, 1990) and other special zero-skew methods (T.-H. Chao. *et.al*., 1992). Also there are other distributions like Bow-tie distribution (Masleid, 2008). Examining these distributions, we can find that diagonal routes are shorter than straight routes as in the case of X-tree and Bow-tie distributions. Shorter routes imply shorter delays and thus resulting in improved speed. The proposed distribution attains a reduction of up to 30% length in clock path.

In this paper, an algorithm which can generate the H-Tree and Bow-tie tree topologies is formulated. The hybrid structure of an H-tree and bow tie demonstrates the reduction of wire length due to the use of diagonal routes. The performance improvement is experimentally analyzed. The reduction in wire length will be reflected in the total area consumed by the routing strategy and thus the total chip size.

The remainder of this paper is organized as follows. Section 2 includes the preliminaries required to understand the paper, Section 3 gives problem formulation. Section 4 is composed of the major components of the algorithm. In Section 5, we present our results. Finally, we give our conclusion in Section 6.

2. Preliminary

The digital circuits are synchronized with the help of clock signals. The basic equation that rules the digital circuit design is

$$CP \geq d_L + t_{SKEW} + t_{SU} + t_{CQ}$$

This expression shows the important relationship between the clock period, the longest path delay, and the clock skew. Most major algorithms in the field of clock network design deals with minimizing the skew and delay. The clock routing step comes after the

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placement step in a digital circuit design flow. To understand the effect of design steps, we need to model the interconnect parasitics that load the clock tree. Interconnect resistance and capacitance are the two parasitics to be modelled.

Interconnect resistance is determined as following.

$$R_i = \frac{\rho L}{WH}$$

Where ρ is the resistivity of metal, L is the interconnect length, W is the interconnect width, and H is the interconnect thickness. Interconnect capacitance is modelled as

$$C_i = K_c(C_{ox} + C_I)$$

Where

$$C_{ox} = \varepsilon_{ox} \frac{WL}{t_{ox}}$$

and

$$C_I = \varepsilon_{ox} \frac{LH}{L_s}$$

Based on the estimates for and, simple and accurate interconnect delay estimates may be calculated using Elmore delay model (R. S. Tsay, 2003). In this, the interconnects are treated as distributed RC trees.

3. Problem Statement

Given the ICs placement, the locations of blockages on the routing layers, the positions of all clock pins on the clock net and the location of clock pad along periphery of the chip, the problem can be defined as following: Construct a clock tree that optimizes the clock skew and wire length, subject to constraints on phase delay and the routing.

Clock tree synthesis is performed before routing other nets, so wire resources are fully available for the clock nets to utilize over the circuit.

Buffers are placed in order to reduce slew. Based on the wire type, the maximum distance between two buffers has to be found using SPICE simulations.

4. Methodology

In this paper, we propose an algorithm which minimizes wire length by using a structure called Bow-Tie along with conventional H-Tree structure. Delay is calculated by Elmore delay model.

4.1 Algorithm

The H-tree algorithm can be implemented using the steps as shown in Figure 1.

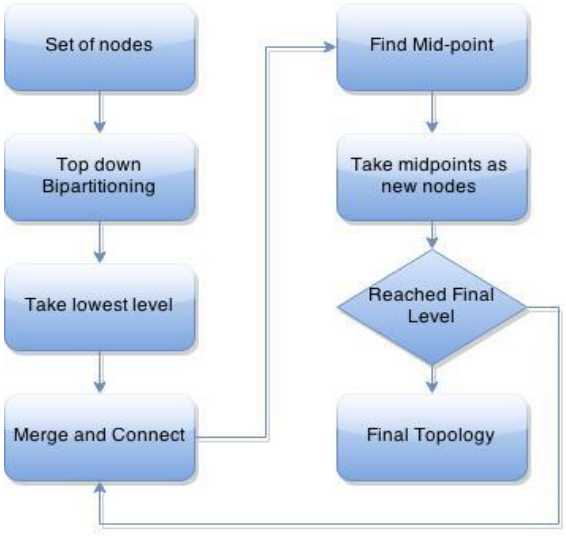

Fig.1 The H-tree Topology Generation Steps

Based on the approach of H -tree, the set of nodes are first partitioned into two equal sets and a connection is established. This is iteratively repeated until single clock sink remains. At each iteration, buffers are inserted based on the maximum distance between buffers using the information from SPICE simulations.

For obtaining bow–tie from H -tree, the wire length for H-tree is closely observed. Halfway from before the splitting point of wire to corner sinks, the diagonal is started and ends at the sinks. 30% reduction in wire length is obtained with this modification.

Fully balanced trees are preferable in clock network synthesis. In asymmetric structures, this obtained by reducing maximum interconnect capacitance.

In our case, to achieve the target, an iterative approach is required to partition the sinks. This naturally includes a sequence of recursive bi-partitioning processes. The procedure for above partitioning is given below.

Procedure Partition (V_i)

Input: V_i ← The group of nodes to be merged in i^{th} iteration.

```
if |Vi| = 2 then
   merge (V1^i, V2^i)
else if |Vi| < 1 then
   return
else if |Vi<4|
   Build Bow-tie with |Vi|-2 edges inserted.
else
   Build H-Tree with |Vi|-2 edges inserted.
   Two groups Vi' and Vi'' are formed.

   partition(Vi')
    partition(Vi'')
 end if
 end if
```

4.2 Layout

To study the effect of wire length on performance, drawing layout of the structures and simulating them is an effective method. The layout will essentially point towards the placement strategies to be followed inorder to reduce the wirelength. This is applicable for clock routes and other wiring networks as well.

5. Experimental Results

The experiments were done in two separate aspects but both pointing to the effectiveness of symmetric/ fractal structures.

We implemented the clock distribution algorithm using MATLAB and simulations were done using SPICE and Cadence Virtuoso for layouts. The SPICE simulation was done on Linux platform. Circuits with 8, 16, 32 and 64 sink points were used for the purpose.

The total H-tree wire length is more than Bow-tie-H-tree hybrid wire length by about 30%. As the level of bow-tie increases, the wire length reduces as well, but at the cost of running time and complexity. Up to 2 level of bow-tie is feasible as per our observations.

Table 1 Experimental parameters

S. No	H-tree			Modified H-tree		
	8	16	32	8	16	32
1	390	780	1560	117	231	467
2	448	650	717	400	509	610

The layouts of some structures were drawn to find the exact impact of wire length on delay or the performance. The drawn layout examples are shown below. H structures show tremendous difference from other structures, i.e. more than 50% difference is obtained.

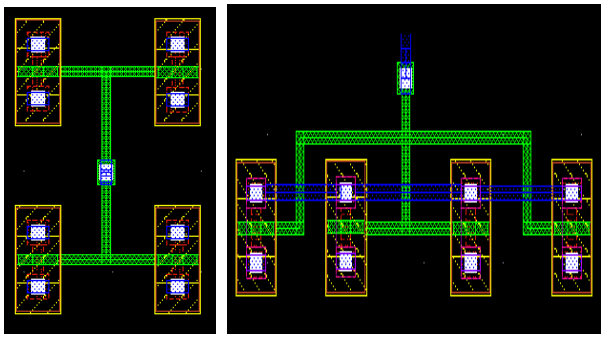

Fig.2 Examples for layout testing for wire length impact

Conclusions

A modified H-tree algorithm based on wire length minimization due to use of diagonal shapes is presented. The algorithm was implemented in MATLAB and simulated using SPICE and a reduction in wire length is obtained. This reduces delay and thus provides an optimization method for symmetric digital circuits. Moreover analysis of layouts were done to prove the effectiveness of H structures. Buffer insertion is recursively that ensures pulse width and latency are maintained. More level of diagonal routes will lead to complexity.

References

E. G. Friedman (2001), Clock distribution networks in synchronous digital integrated circuits, *Proceedings of the IEEE*, vol. 89, no. 5, pp. 665–692.

M. A. Franklin and D. F. Wann (1982), Asynchronous and clocked control structures for vlsi based interconnection networks, in *ACM SIGARCH Computer Architecture News*, vol. 10, pp. 50–59.

D. F. Wann and M. A. Franklin (1983), Asynchronous and clocked control structures for VLSI based Interconnection networks, *IEEE Transactions on Computers*, vol. 100, no. 3, pp. 284–293.

F. Anceau (1982), A synchronous approach for clocking vlsi systems, *IEEE Journal of Solid-State Circuits*, vol. 17, no. 1, pp. 51–56.

R. P. Masleid (2008), Bow tie clock distribution, *US Patent* App. 12/336,380.

R. P. Masleid and S. Pitkethly (2008), Double diamond clock and power distribution, *US Patent* 7,689,963.

P. Ramanathan and K. G. Shin (1989), A clock distribution scheme for non-symmetric vlsi circuits, in *Proc. IEEE Int. Conf. Computer Aided Design*, pp. 398–401.

T.-H. Chao, Y.-C. Hsu, J.-M. Ho, and A. Kahng (1992), Zero skew clock routing with minimum wirelength, Circuits and Systems II, *IEEE Transactions on Analog and Digital Signal Processing* , vol. 39, no. 11, pp. 799–814.

H. Bakoglu, J. Walker, and J. Meindl (1986), A symmetric clock-distribution tree and optimized high-speed interconnections for reduced clock skew in ulsi and wsi circuits, in *Proc. IEEE Int. Conf. Computer Design*, pp. 118–122.

J. Burkis (1991), Clock tree synthesis for high performance asics, ASIC Conference and Exhibit, *Fourth Annual IEEE International Proceedings.*

J. P. Fishburn, Clock skew optimization (1990), *IEEE Transactions on Computer*s, vol. 39, no. 7, pp. 945–951.

M. Edahiro (1990), A clock net reassignment algorithm using Voronoi diagram, *IEEE International Conference on Computer- Aided Design, Digest of Technical Papers*, pp. 420–423.

S. Dhar, M. A. Franklin, and D. Wann, Reduction of clock delays in vlsi structures (1984), in Proc. IEEE Intl. Conf. on Computer Design, pp. 778–783.

A. L. Fisher and H. Kung (1982), Synchronizing large systolic arrays, Technical Symposium East, *International Society for Optics and Photonics*, pp. 44–52 .

H. B. Bakoglu (1990), Circuits, interconnections, and packaging for VLSI.

Y. Chen and D. Wong (1996), An algorithm for zero-skew clock tree routing with buffer insertion, in *European Design and Test Conference, IEEE Proceedings*, pp. 230–236.

R.-S. Tsay (2003), Exact zero skew, in The *Best of ICCAD*, *Springer*, pp. 509–520.

S. Pullela, N. Menezes, and L. T. Pillage (1993), Reliable non-zero skew clock trees using wire width optimization, in *Proceedings of the 30th international Design Automation Conference*, *ACM*, pp. 165–170.