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Research Article

Sub word Partitioning and Signal Value based Clock gating Scheme for Low Power VLSI Applications

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Abstract

The low power optimization techniques are very crucial for next generation wireless communication and battery powered signal processing applications. Several low power optimization techniques at circuit level and device level were implemented in past two decades to achieve low power design. However the continuously growing low power demand motivates researchers to evolve even low power designs. The architecture level low power optimization is possible for signal processing and in communication applications, considering the dynamically fluctuating signal value. The work given here presents the subword partitioning and signal value based dynamic clock gating method to achieve low power implementation without compromising on the performance. A scalable subword based clock gating scheme is presented here. A novel no-information based detection scheme is used to power down sequential and combinational logic specific to each subword. A four bit subword register is used for validating the proposed low power scheme. The circuit is designed at schematic level and extracted netlist is simulated with 130 nm CMOS model file. The simulation results for clock gating scheme demonstrated average power optimization of 21% when compared to simulation results without clock gating scheme. The future work is aimed to achieve higher power savings for developing combinational logic with power gating feature.

Keywords: *Low power, data driven clock gating, dynamic power, CMOS 130 nm, CMOS, average power analysis*

1. Introduction

The low power optimization techniques are very crucial for next generation wireless communication and battery powered signal processing applications. Several low power optimization techniques at circuit level and device level were implemented in past two decades to achieve low power Very Large Scale Integration (VLSI) designs. However the continuously growing low power demand motivates researchers to evolve even low power designs. The architecture level low power optimization is possible for signal processing and the communication applications considering the dynamically fluctuating signal value. The work given here presents the detailed architecture for sub word partitioning and signal value based dynamic clock gating method to achieve low power implementation without compromising on the performance.

1.1 Static Vs Dynamic Power

The amount of energy consumed per operation and the heat dissipated by the circuit are determined by the power consumption of a design. A great number of critical design decisions, like the battery lifetime, supply-line sizing, power supply capacity, packing and cooling requirements are being influenced by the above factors. Power dissipation is an important property of a design that affects feasibility, cost, and reliability. However, the number of circuits that can be integrated onto a single chip, and how fast they are allowed to switch are determined by their high-performance computing, power consumption limits and the heat removal system (Jan M. Rabaey).

In present era of increasing mobile computing applications, for the amount of energy stored in battery, the achievable number of computations directly depend on power consumption of Integrated Circuits (ICs). Depending upon the design problem, different dissipation measures have to be considered. For instance, the peak power P_{peak} is important when studying supply-line sizing. While addressing cooling or battery requirements, one is predominantly interested in the average power dissipation P_{av}.

The below equations determines the peak power and average power in general.

$$P_{Peak} = i_{Peak} V_{Supply} = \max [P(t)] \quad (1)$$

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$$P_{av} = \frac{1}{T}\int_0^T P(t)dt = \frac{V_{Supply}}{T}\int_0^T i_{Supply}(t)dt \quad (2)$$

Where, p(t) is the instantaneous power, i_{supply} is the current being drawn from the supply voltage V_{supply} over the time interval in range [0, T], and i_{peak} is the maximum value of i_{supply} over that interval. Power dissipation of the circuit is given in equation 3

$$P_{Total} = P_{Dynamic} + P_{static} \quad (3)$$

The power dissipation in digital circuits is classified into static and dynamic. The power dissipated when the circuit is powered up with no input or output signals changing their values is called static power. Dynamic power is the power consumed as a result of changing node voltages and resulting charging and discharging cycles of associated node capacitances.

In current CMOS circuits (Michael Keating, 2007), static power consumption is mainly due to leakage current and this is predominant in memories.

$$P_{Static} = I_{Static} V_{dd} \quad (4)$$

Equation (4), describes the individual components of static power. Where, V_{dd} is the supply voltage and I_{static} is the total current flowing through the device. The prime advantage of CMOS technology is low static power. However, as devices are scaled, any reduction in gate oxide thickness resulted in increased probability of tunneling and also increase of larger and larger leakage currents. Researchers are focusing on improvising MOS devices to reduce leakage power in them. With growing usage of CMOS VLSI in digital and RF designs, the dynamic power component is the dominant power component to be optimized. The first and primary source of dynamic power consumption is switching activity in input and output, which is the power required to charge and discharge the output capacitance on output gate.

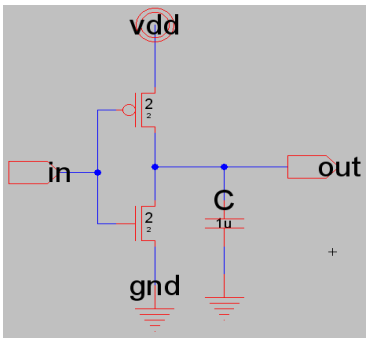

Fig.1 Transition in inverter input leading to switching Power

Dynamic power is the function of the transients and transients is internally a function of input signals. The sum of transient power consumption ($P_{transient}$) and capacitive load power (P_{cap}) consumption is due to dynamic power dissipation in CMOS circuitry. Amount of power consumed when the device toggles its logic states from logic 0 to 1 or vice versa is represented by $P_{transient}$. Charging and discharging of the load capacitance is due to consumption of capacitive load power. Hence the total dynamic power can be represented as in equation (5).

$$P_{Dynamic} = P_{Cap} + P_{Transient} = (C_L + C)\, V_{dd}^2\, f\, \alpha \quad (5)$$

Where, C_L is the total load capacitance and C is the internal capacitance of the CMOS gate. Where, f is the frequency of operation, and α is the activity factor related to switching activity which is happening on the net connected C_L and C. The higher the number of switching events, the resulting dynamic power consumption is higher. The static component on the other hand is present even when no switching occurs and is caused by static conductive paths between the supply rails or by leakage currents. It is always present, even when the circuit is in stand-by. Minimization of this consumption source is a worthwhile goal.

The propagation delay is mostly determined by the speed at which a given amount of energy can be stored on the gate capacitors. The faster the energy transfer (or the higher the power consumption), the faster the gate and vice versa. For a given technology and gate topology, the product of power consumption and propagation delay is called power-delay product (or PDP) which is generally a constant. PDP can be considered as a quality measure for a switching device. The PDP is simply the energy consumed by the gate per switching event. To measure the PDP of a logic family, ring oscillator is the circuit of choice.

2. Reducing dynamic power dissipation

The dynamic power saving can be attempted by glitch reduction and clock gating. The following section describes these methods.

2.1 Glitch Reduction

A major source of dynamic power resulting from unwanted capacitor charging and discharging cycles in large data paths is due to spurious transitions caused by glitch propagation. Glitches result when input of a combinational logic circuit is driven by inputs, which has mismatched delays. In large combinational blocks such as array multipliers, transitions happen in wave as the primary input changes ripple through the logic (Jan M. Rabaey). Glitch transitions can be reduced by enabling the logic once the inputs are settled. In self timed gating approach, each computational logic block is portioned into smaller blocks and distinct phases. Several VLSI gate level synthesis tools use these methods for glitch reduction.

2.2 Clock gating

Clock gating is the main technique used by designers for power reduction at gate-level synthesis (Priya

Singh, 2014). Clock gating provides mechanism to disable the clock for sequential logic circuits. Simplest clock gating scheme will disable the clock when the inputs are unaltered between previous clock cycle and present clock cycle. If there is no activity required by the current block then also clock can be disabled. Usually the clock is gated with enable signal for implementing clock gating capable flip-flop.

The dynamic power consumption is considerably reduced with clock gating, as the charging and discharging of capacitances are avoided for conditions where input is same. There are (M. Shreya, 2014) different types of clock gating schemes for digital circuits. The methods of designing low power circuits with clock gating is different for combination logic and sequential logic (K. Hariharan, 2012). In the present work, clock gating is based on novel no-information detection scheme in signal processing applications. The scheme has main advantage of low area over head when compared to typical comparator based clock gating scheme.

3. Proposed clock gating architecture

Among several available clock gating techniques only few are suitable for signal processing applications on FPGAs. The work presented at (Wilmer, 2014) proposes Look-Ahead Clock Gating (LACG). It computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends.

In signal processing applications the registers are driven with data coming from sensors through Analog to Digital Converters (ADCs). In such applications even under no signal conditions due to random noise few LSB bits always change in the input signal. The drawback of conventional clock gating schemes in signal processing applications is that, the gating signal is high. Hence, even clock gating scheme is implemented in hardware, power saving cannot happen, as the gate enable is high. In addition to this draw back there is another limitation for using clock gating in signal processing applications which is, the area overhead due to comparator before every register.

In this paper sub word based architecture is proposed to detect the presence of the information in the magnitude bits in a particular sub word out of a given word. The bus with n+1 bits carrying a signal is considered, which uses 2's complement representation. The Fig. 2, explains the sub word representation of the n+1 bit signal, where each sub word has m= (n/p) bits. The n bit magnitude word is divided into p sub words, each representing a particular part in the full dynamic range of signal.

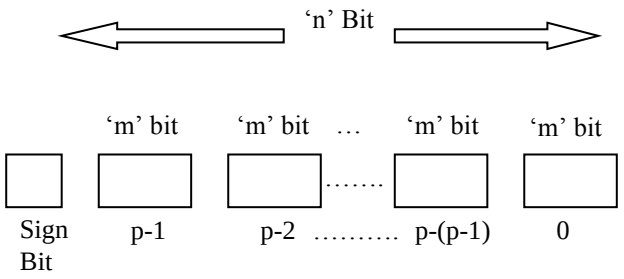

Fig. 2 (n+1) bit register represented as sub words

The presence of information is checked in each sub word to generate the enable for clock gating . The signal X represented with n+1 bits can be described as in equation(6). The sub word based representation of same signal is given in equation (7).

$$X = \{ b_n, b_{n-1}, b_{n-2} \ldots\ldots\ldots b_1, b_0 \} \quad (6)$$

$$X = \{ b_n, \{b_{m-1}, \ldots\ldots\ldots b_0 \}_{p-1}, \{b_{m-1}, \ldots\ldots\ldots b_0 \}_1, \{b_{m-1}, \ldots\ldots\ldots b_0 \}_0, \} \quad (7)$$

The NO Information (NOI) flag at i^{th} sub word ($0 < i < p-1$) is considered as 1 when all the m bits in sub word $\{b_{m-1}, \ldots\ldots\ldots b_0 \}$ are equal to sign bit b_n and also all the high significant j^{th} ($i+1 < j < p-1$) sub words has NIO flag 1. The no information flag at i^{th} stage can be computed by using the OR gate in case of positive signals and NAND gate for negative numbers. In case of signal changing from negative to positive and vice versa the NOI flag must be set to zero. The condition of no information in a subword can be considered for two combinations of inputs.

The two input combinations where the proposed clock gating scheme can lead to power saving are as below.

- The first condition is En_MSSW is 0 and sign bit 0 and all the inputs are 0's.
- The second condition is the En_MSSW is 1 and sign bit is 1 and all the inputs are 1's.

The Fig. 3, has the logic circuit for generating the enable for clock of i^{th} sub word. The 0th sub-word consist the least significant bits hence it will always contain the information even for smaller magnitudes of the data in the register. The circuit in Fig.3 is optimal gate level implementation of enable generation. The En_MSSW is a enable coming from $(i+1)^{th}$ subword stage, the sign is a sign bit for entire word. The circuit considers 4 bit subword size. The d3,d2,d1,do is a input to the register(D-fliflops).the enable out EN_i generates which is enable for i^{th} stage of subword. This enable will be gated along with clock and is applied to D-flipflop.

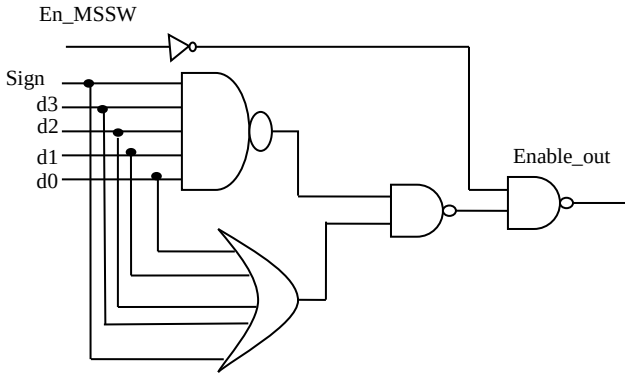

Fig. 3 EN_i generation for i^{th} sub word

Figure 4 shows general RTL implementation of any circuit with proposed subword based clock gating scheme.

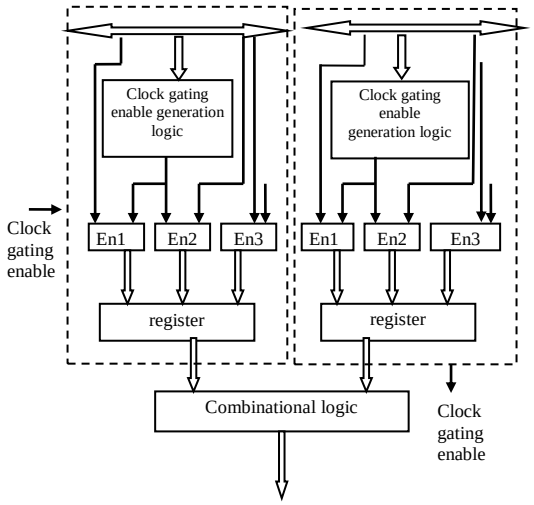

Fig.4 Pipe-lined combinational logic after subword based clock gating scheme

The Figure shows the clock gating logic on two registers each with 3 sub words. The outputs of two registers can be given to combinational logic. The figure 5 shows clock gated D-flipflop where the enable is driven by the proposed subword based clock gating scheme.

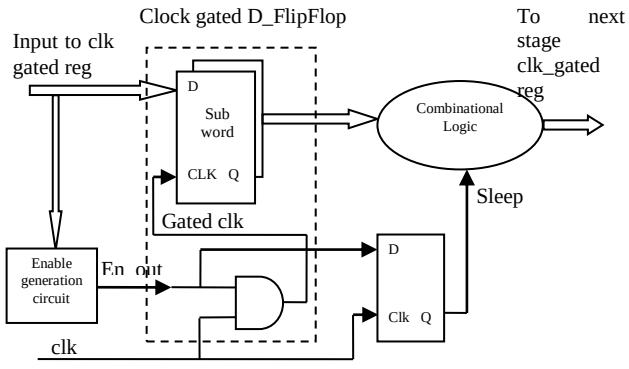

Fig.5 Clock gated D-flipflop with proposed subword based enable generation

The gate level implementation of enable generation circuit is given in figure 3. This enable output becomes input to the and gate used for clock gating. The other input to and gate is clock coming from the clock tree. The and gate output which is gated clock fed to the D-fliflop clock input. The D-flipflop input D is same input which is applied to the enable generation circuit. The D-flipflop output Q is fed to the combination logic circuit which is controlled by this sleep signal. The signal sleep is one cycle delayed version of enable output. This is required because the Q output takes the value of D after one clock cycle only. Hence the enabling disabling of the combinational logic must be applied after one clock cycle.

When the signal sleep is equal to 1 the combinational logic works in a normal way. Whereas when the signal sleep is equal to 0, then the combinational logic turns into sleep mode. This power gating (sleep mode) ensures that even the leakage power in combinational logic is reduced during the sleep mode.

The final output of figure 5 can be applied to the next stage clock gating register. In the present work the power analysis of clock gated register along with the enable generation circuit are studied. Since the power reduction in combinational logic is under sleep mode which is evident from several other researchers works. This is applicable for any type combinational circuit.

4. Clock gated Delay Flip Flop (DFF)

Figure 6 shows high level schematic of clock gated D-flipflop.

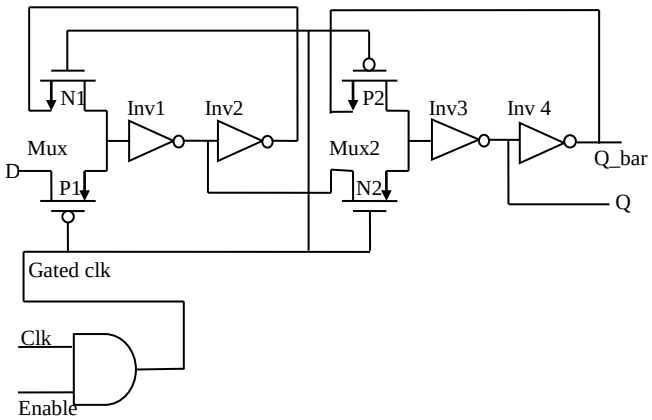

Fig.6 High level schematic for clock gated register

The master-slave flip flop is basic FF architecture which is used in Gate-Diffusion Input (GDI) Multiplexers, is shown with clock gating feature in Fig. 6. A pair of latches comprising a GDI multiplexer and a cross-coupled pair of inverters are used. The Mux1 is and Mux2 are realized by P1&N1 and P2&N2 pairs of transistors respectively. The selector of first multiplexer is connected to the system clock (Clk) and its inputs are connected to the FF input (D) and the

feedback loop. The inverted signal is applied to the input to the second latch, with the feedback loop connected to the opposite input of the second multiplexer (Mux2). This creates a rising edge type Delay FF with a reduced Propagation delay due to the single inversion required to produce output. Cell sizing can be done to optimize between speed and area constraints.

5. Clock gated subword register with 130 nm CMOS

The figure 7 shows 4 bit register with the proposed subword based clock gating scheme.

The inputs d3, d2, d1, d0 is a 4 bit subword which is input to the register. Sign is the MSB of the entire signal. The En_MSSW is a enable coming from $(i+1)^{th}$ subword stage.

The information (INFO) Detector is the enable generation circuit, whose detailed logic level implementation is presented in Figure 3. The En generated is applied to En input of D Flip-Flop. The high level schematic of clock gated DFF is given in figure 6. The q3, q2, q1, q0 is the output of the 4 bit clock gated register.

Figure 8 gives the schematic which is developed using electric VLSI tool with CMOS logic family and transistor for gated D-flipfllop. figure 9 has schematic of enable generator circuit. Figure 10 shows schematic of complete 4 bit subword register with enable generation logic. Using Electric VLSI design tool, the spice netlist of the schematic is generated. The Taiwan Silicon Manufacturing Company (TSMC) IC fabrication measured process file (model file) for 130 nm CMOS process is used for SPICE simulation. The results are presented in the next section.

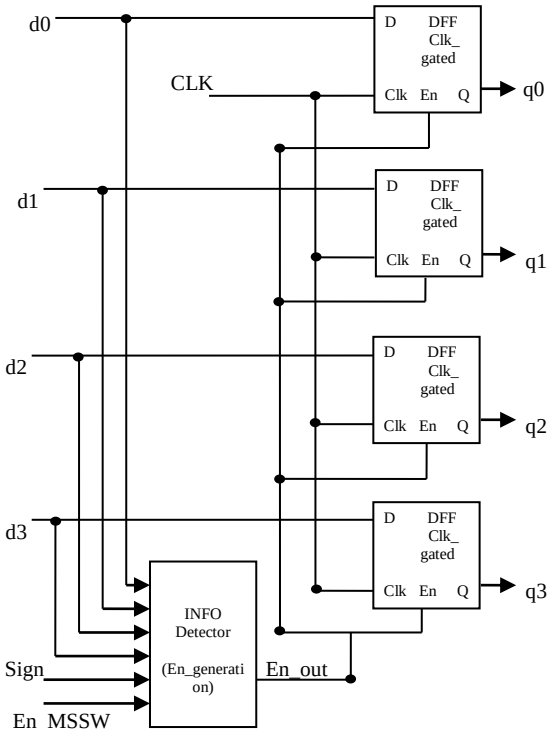

Fig.7 4 bit register with clock gating

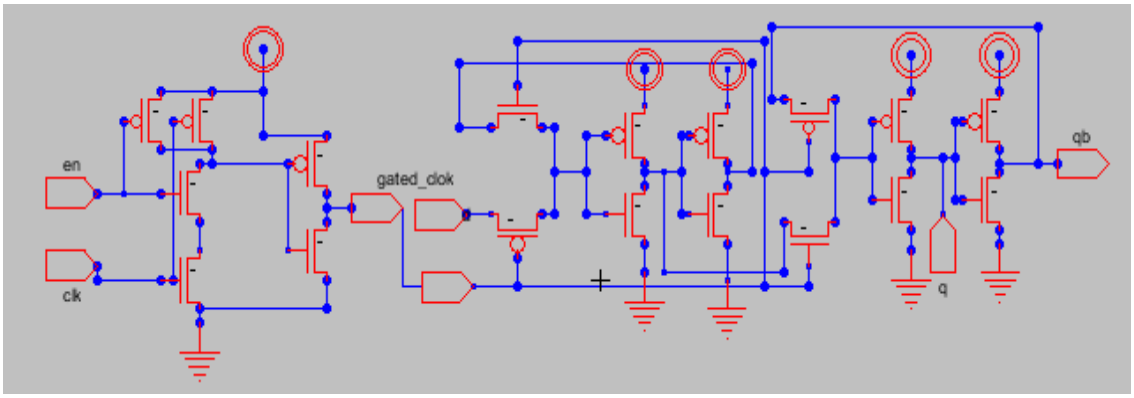

Fig.8 Schematic of clock gated D-flipflop using 130nm CMOS technology

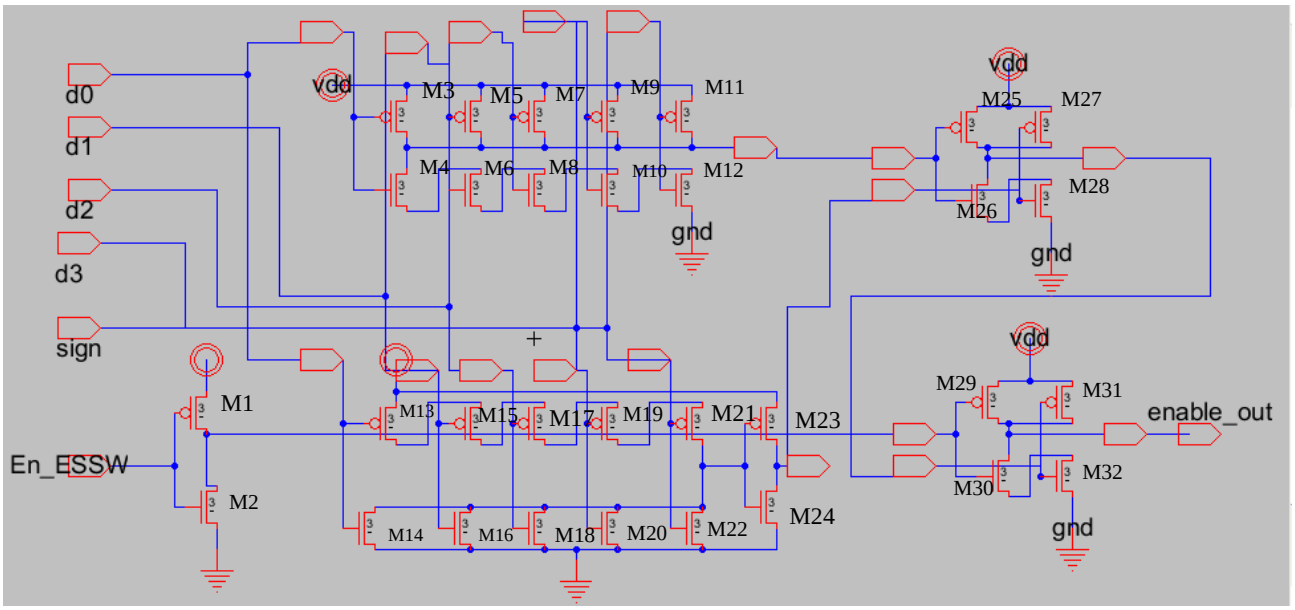

Fig.9 Schematic of enable generation circuit using 130nm CMOS technology

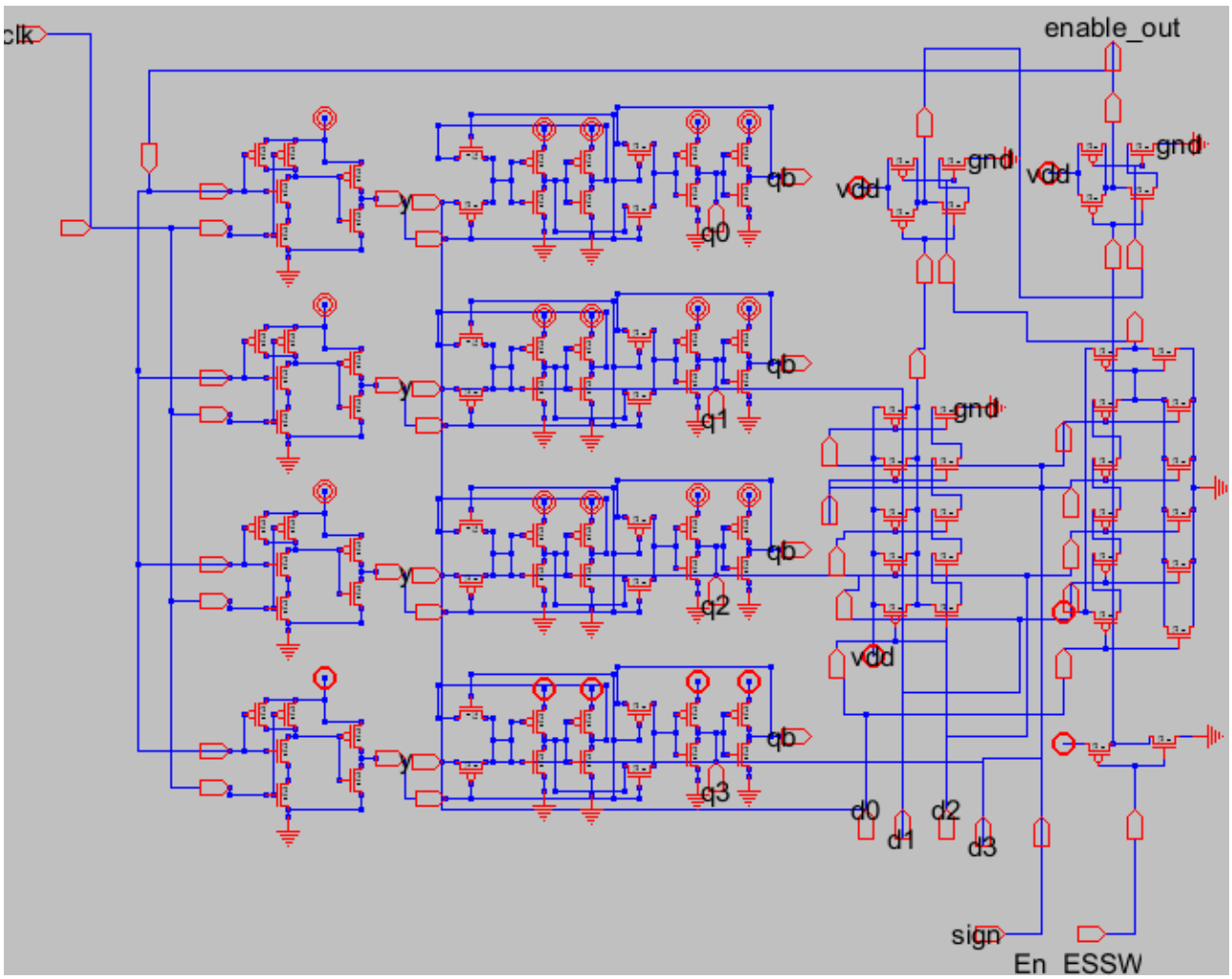

Fig.10 Schematic of clock gated 4 bit subword register using 130nm CMOS technology

Fig 9 shows the enable generation circuit for the clock gating scheme, implemented as per the design illustrated in Fig 3. The circuit consists total 32 transistors. The logic gates implemented are 5 input

NAND gate, 5 input OR gate, 2 input NAND gate and inverters. Transistors M1 and M2 are connected as inverter, which takes input from En_MSSW and the inverted output of this inverter is one of the two input to NAND gate. The transistors M3,M4,M5.M6,M7, M8,M9,M10,M11,M12 transistors are connected as the 5 input NAND gate. The transistors M13,M14,M15,M16,M17,M18,M19,M20,M21,M22,M23, M24 are used to realize 5 input OR gate. The remaining transistors realize 2 two input NAND gates to generate the final enable for clock gating.

The Fig 10, is the transistor level schematic of developed, 4 bit clock gated subword register. The design consists of four 1 bit clock gated registers which are driven by common gated clock. The high level block diagram given at Fig 7, explains the functionality of this module. Inputs for this clock gated register are clock, D[3:0], enable and outputs are Q[3:0], Q_bar[3:0]. The enable generation circuit explained above generates enable for this module.

6. Simulation results

Simulation at two different levels is performed for verifying the developed scheme. The logic correctness of enable generation circuit is initially verified with the VHDL simulation. The Mentor graphics HDL simulator, Modelsim tool is used and waveform output for the enable generation circuit is given in figure 11.

Test bench developed for considering the 64 possible combinations for six input combinational logic. The results are verified to produce output enable zero for two combinations and high for remaining 62 combinations. Further the results are verified with SPICE simulator for enable generation circuit. The results are verified and shown in Figure 12.

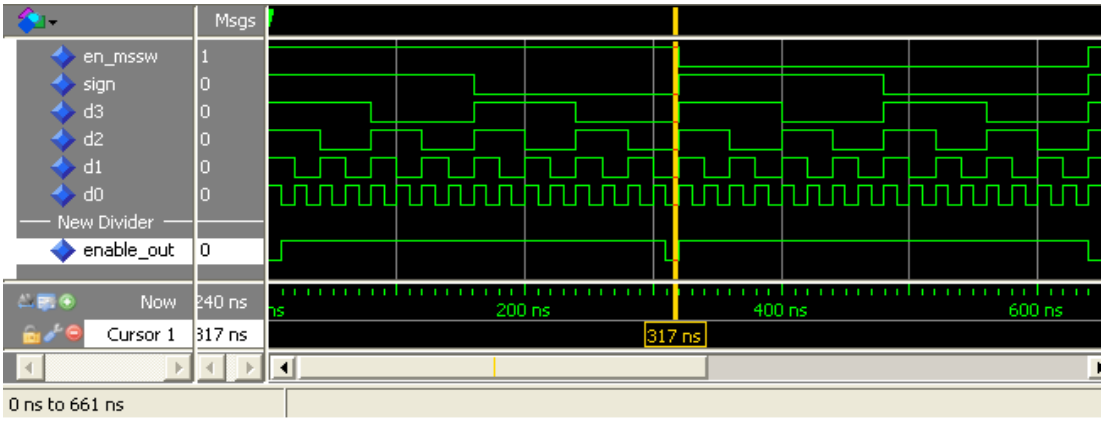

Fig.11 VHDL simulation result for enable generation circuit

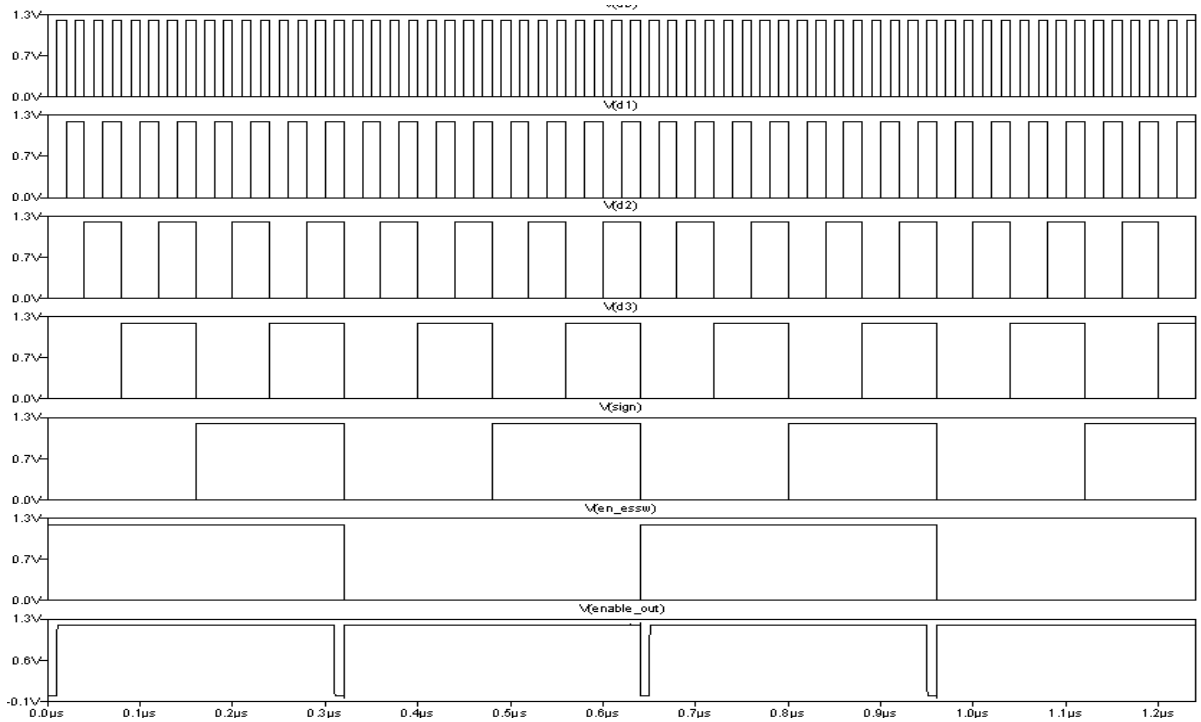

Fig.12 Spice simulation results for enable generation circuit

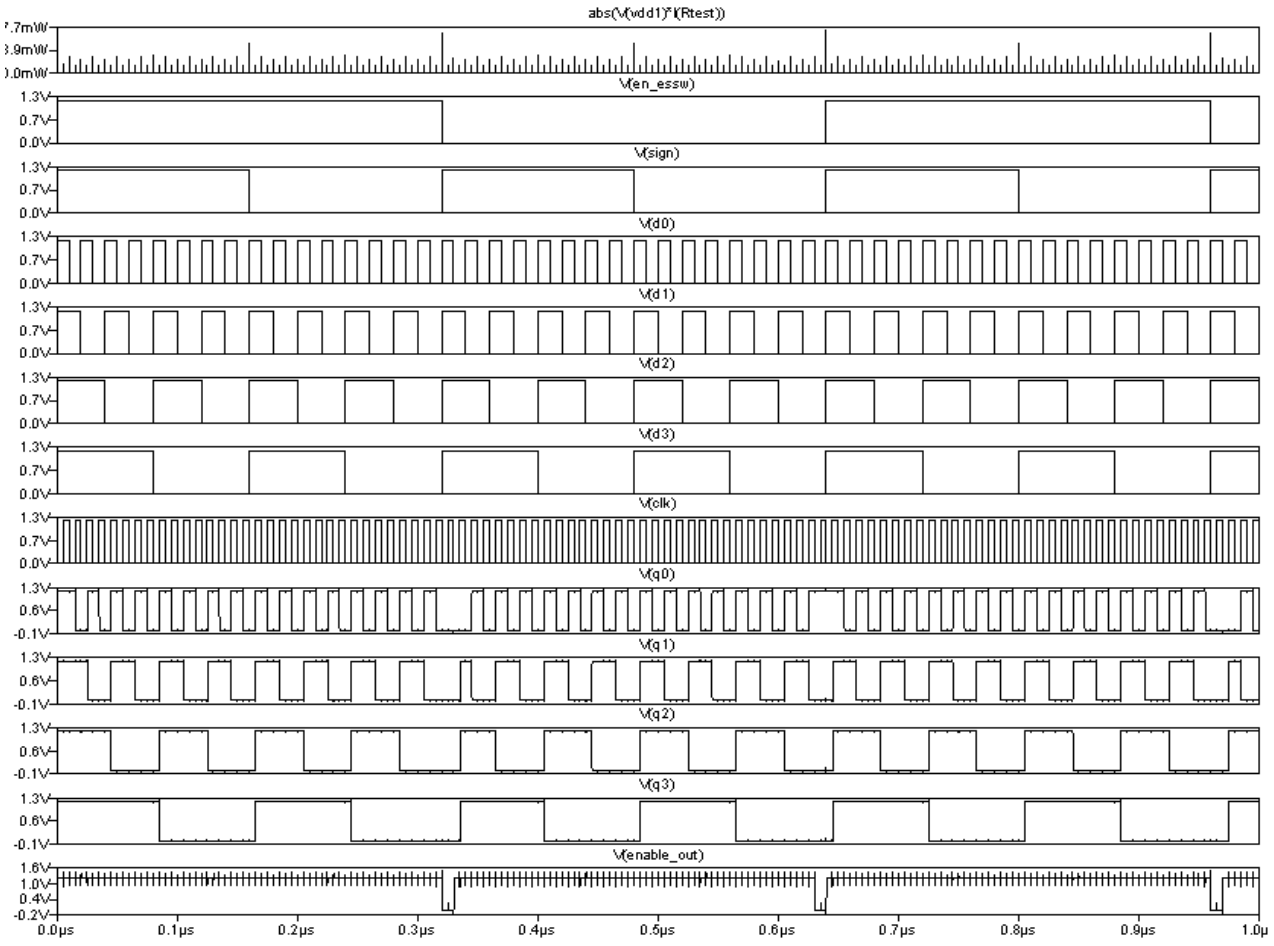

Fig.13 Spice simulation results for 4 bit subword register

Table 1 Power Analysis

Input condition			NOI % of sim time	Power (uw)	Power saving (%)
En_MSSW	Sign	d3d2d1d0			
0	0	0000	0	7.6678	0
1	0	1111	0	8.2305	0
0	0	0000	10	7.1352	7
1	0	1111	10	7.9601	3
0	0	0000	20	6.6732	13
1	0	1111	20	7.7083	6
0	0	0000	30	6.3007	18
1	0	1111	30	7.5991	7
0	0	0000	40	5.9276	22
1	0	1111	40	7.3222	11
0	0	0000	50	5.5224	28
1	0	1111	50	7.0674	14

From Figure 12, it can be observed that the enable output high for all the cases where the subword is having information and becomes 0 only in the two cases where there is no information.

Figure 13 has simulation results for entire 4-bit subword based register with clock gating scheme. Results verified by checking the updation of q3, q2, q1 and q0 on rising edge of clock based on d3, d2, d1 and d0 respectively.

Average power analysis is performed on the developed circuit and results are compared with simple 4 bit register without clock gating scheme. Since the power saving happens under conditions of no-information (NOI) cases only, the analysis need to be carried out considering the probability of such input conditions.

Table 1 shows power analysis for power saving at different percentages of NOI input combinations. For each probability case the power saving in two input

combinations are shown separately. Considering the average of both the case for 50% probability of NOI conditions the results showed 21% for power saving.

In signal processing applications when the input signal is small in value, the most significant subwords will be in NOI condition only. Hence the assumption of 50% criteria is applicable for the envisaged usage of the proposed clock gating scheme.

Conclusions

Scalable architecture for signal value based clock is presented in this research work. The signal width is divided into subwords where each subword is driven for separate clock gating signal. The relationship between clock gating signals of adjacent subwords is fully utilized in realizing area efficient clock gating scheme. By reducing the area overhead for clock gating logic, the penalty on increased static and leakage power is less when compared to saved dynamic power. SPICE Simulation results demonstrate up to 21% of power saving with the proposed clock gating scheme.

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