

Research Article

Cascade Converter based Generalized UPQC Condition System

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Abstract

In this paper, a new configuration of a UPQC called the multiconverter unified power-quality conditioner (MC-UPQC) is presented. The system is extended by adding a series-VSC in an adjacent feeder. The proposed topology can be used for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system is also capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations.

Keywords: UPQC, VSC, MC-UPQC

1. Introduction

With increasing applications of nonlinear and electronically switched devices in distribution systems and industries, power-quality (PQ) problems, such as harmonics, flicker, and imbalance have become serious concerns. In additional lightning strikes on transmission lines, switching of capacitor banks, and various network faults can also cause PQ problems, such as transients, voltage sag/swell, and interruption. On the other hand, an increase of sensitive loads involving digital electronics and complex process controllers requires a pure sinusoidal supply voltage for proper load operation.

In order to meet PQ standard limits, it may be necessary to include some sort of compensation. Modern solutions can be found in the form of active rectification or active filtering. A shunt active power filter is suitable for the suppression of negative load influence on the supply network, but if there are supply voltage imperfections, a series active power filters may be needed to provide full compensation. In recent years, solutions based on flexible ac transmission systems (FACTS) have appeared. The application of FACTS Concepts in distribution systems have resulted in a new generation of compensating devices. A unified power-quality conditioner (UPQC) is the extension of the unified power-flow controller (UPFC) concept at the distribution level. It consists of combined series and shunt converters for simultaneous compensation of voltage and current imperfections in a supplyfeeder. Recently, multiconverter FACTS devices, such as an interline power-flow controller (IPFC) and the generalized unified power-flow controller (GUPFC) are introduced. The aim of these devices is to control the power flow of

multiline or a sub network rather than control the power flow of a single line by, for instance, a UPFC.

Furthermore, by using the multiline-management capability of the GUPFC, active power flow on lines cannot only be increased, but also be decreased with respect to operating and market transaction requirements. In general, the GUPFC can be used to increase the transfer capability and relieve congestions in a flexible way. This concept can be extended to design multiconverter configurations for PQ improvement in adjacent feeders. For example, the interline unified power-quality conditioner (IUPQC), which is the extension of the IPFC concept at the distribution level, has been proposed in . The IUPQC consists of one series and one shunt converter. It is connected between two feeders to regulate the bus voltage of one of the feeders, while regulating the voltage across a sensitive load in the other feeder. In this configuration, the voltage regulation in one of the feeders is performed by the shunt-VSC. However, since the source impedances very low, a high amount of current would be needed to boost the bus voltage in case of a voltage sag/swell which is not feasible .It also has low dynamic performance because the dc-link capacitor voltage is not regulated.

2. Proposed MC-UPQC system

2.1 Circuit Configuration

The single-line diagram of a distribution system with an MC-UPQC is shown in Fig.

As shown in this figure, two feeders connected to two different substations supply the loads L1 and L2. The MC-UPQC is connected to two buses BUS1 and BUS2 with voltages of u_{t1} and u_{t2s} respectively.

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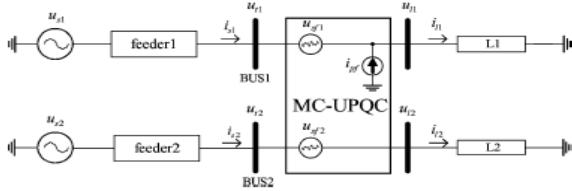


Fig 2.1 Single-line diagram of a distribution system with an MC-UPQC

The shunt part of the MC-UPQC is also connected to load L1 with a current of i_{11} . Supply voltages are denoted by u_{s1} and u_{s2} while load voltages are u_{l1} and u_{l2} finally, feeder currents are denoted by i_{11} and i_{12} and load currents are i_{l1} and i_{l2} , Bus voltages u_{t1} and u_{t2} and u_{l1} and u_{l2} are distorted and may be subjected to sag/swell. The load L1 is a nonlinear/sensitive load which needs a pure sinusoidal voltage for proper operation while its current is non-sinusoidal and contains harmonics. The load L2 is a sensitive/critical load which needs a purely sinusoidal voltage and must be fully protected against distortion, sag/swell, and interruption. These types of loads primarily include production industries and critical service providers, such as medical centers, airports, or broadcasting centers where voltage interruption can result in severe economic losses or human damages.

2.2. MC-UPQC Structure

The internal structure of the MC-UPQC is shown in Fig.

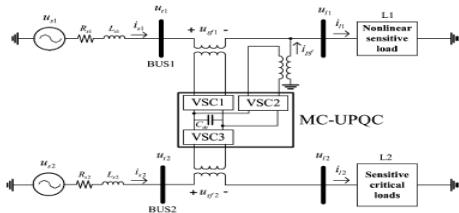


Fig 2.2 Typical MC-UPQC used in a distribution system.

It consists of three VSCs (VSC1, VSC2, and VSC3) which are connected back to back through a common dc-link capacitor. In the proposed configuration, VSC1 is connected in series with BUS1 and VSC2 is connected in parallel with load L1 at the end of Feeder1. VSC3 is connected in series with BUS2 at the Feeder2 end. Each of the three VSCs in Fig. 2 is realized by a three-phase converter with a commutation reactor and high-pass output filter as shown in Fig.

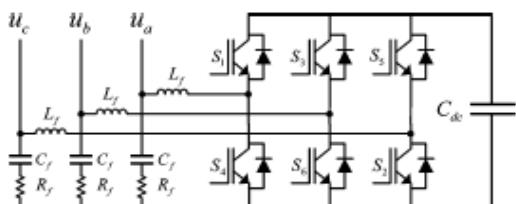


Fig 2.3 Schematic structure of a VSC

The commutation reactor L_f and high-pass output filter (R_f, C_f) are connected to prevent the flow of switching harmonics into the power supply. As shown in Fig, all converters are supplied from common dc-link capacitor and connected to the distribution system through a transformer. Secondary (distribution) sides of the series-connected transformers are directly connected in series with BUS1 and BUS2, and the secondary (distribution) side of the shunt-connected transformer is connected in parallel with load L1.

The aims of the MC-UPQC shown in Fig are

- to regulate the load voltage U_{L1} against sag/swell and disturbances in the system to protect the nonlinear/sensitive load L1;
- to regulate the load voltage (u_{l2}) against sag/swell, interruption, and disturbances in the system to protect the sensitive/critical load L2;
- to compensate for the reactive and harmonic components of nonlinear load current (i_{11}) .
- In order to achieve these goals, series VSCs (i.e., VSC1 and VSC3) operate as voltage controllers while the shunt VSC (i.e., VSC2) operates as a current controller.

3. Power-Rating Analysis of the MC-UPQC

The power rating of the MC-UPQC is an important factor in terms of cost. Before calculation of the power rating of each VSC in the MC UPQC structure, two models of a UPQC are analyzed and the best model which requires the minimum power rating is considered. All voltage and current phasors used in this section are phase quantities at the fundamental frequency. There are two models for a UPQC—quadrature compensation (UPQC-Q) and in phase compensation (UPQC-P). In the quadrature compensation scheme, the injected voltage by the series-VSC maintains a quadrature advance relationship with the supply current so that no real power is consumed by the series VSC at steady state. This is a significant advantage when UPQC mitigates sag conditions. The series VSC also shares the voltampere reactive (VAR) of the load along with the shunt-VSC, reducing the power rating of the shunt-VSC.

Fig. shows the phasor diagram of this scheme under a typical load power factor condition with and without voltage sag.

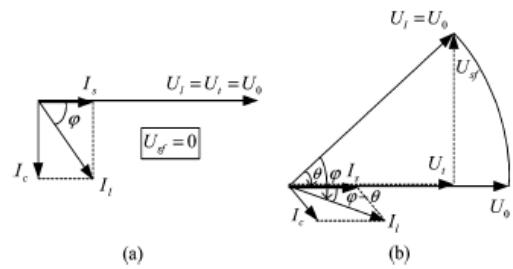


Fig 3.1 Phasor diagram of quadrature compensation
(a) Without voltage sag. (b) With voltage sag

When the bus voltage is at the desired value ($u_t = u_i = u_0$), the series-injected voltage (u_{sf}) is zero [Fig.(a)]. The shunt VSC injects the reactive component of load

Current, resulting in unity input-power factor. Furthermore, the shunt VSC compensates for not only the reactive component, but also the harmonic components of the load current I_c . For sag compensation in this model, the quadrature series voltage injection is needed as shown in Fig.(b).

Fig.(b). the shunt VSC injects I_c in such a way that the active power requirement of the load is only drawn from the utility which results in a unity input-power factor. In an in phase compensation scheme, the injected voltage is in phase with the supply voltage when the supply is balanced. By virtue of in phase injection, series VSC will mitigate the voltage sag condition by minimum injected voltage. The phasor diagram of Fig. explains the operation of this scheme in case of voltage sag.

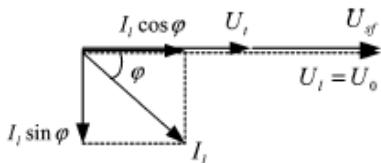


Fig 3.2 Phasor diagram of in phase compensation (supply voltage sag)

A comparison between in phase (UPQC-P) and quadrature (UPQC-Q) models is made for different sag conditions and load power factors in [13]. It is shown that the power rating of the shunt-VSC in the UPQC-Q model is lower than that often UPQC-P, and the power rating of the series-VSC in the UPQC-P model is lower than that of the UPQC-Q for a power factor of less than or equal to 0.9. Also, it is shown that the total power rating of UPQC-Q is lower than that of UPQC-P where the VAR demand of the load is high.

As discussed in Section II, the power needed for interruption compensation in Feeder2 must be supplied through the shunt VSC in Feeder1 and the series VSC in Feeder2. This implies that power ratings of these VSCs are greater than that of the series one in Feeder1. If quadrature compensation in Feeder1 and in phase compensation in Feeder2 are selected, then the power rating of the shunt VSC and the series VSC (in Feeder2) will be reduced. This is an important criterion for practical applications. Based on the aforementioned discussion, the power-rating calculation for the MC-UPQC is carried out on the basis of the linear load at the fundamental frequency.

The parameters in Fig. are corrected by adding suffix 1, indicating Feeder1, and the parameters in Fig. are corrected by adding suffix 2, indicating Feeder2. As shown in Figs. 6 and 7, load voltages in both feeders are kept constant at U_0 regardless of bus voltages variation, and the load currents in both feeders are assumed to be constant at their rated values (i.e., I_{o1} and I_{o2} , respectively)

$$U_{l1} = U_{l2} = U_0$$

$$I_{l1} = I_{o1}$$

$$I_{l2} = I_{o2}$$

The load power factors in Feeder1 and Feeder2 are assumed to be $\cos\psi_1$ and $\cos\psi_2$ and the per-unit sags, which

must be compensated in Feeder1 and Feeder2, are supposed to be x_1 and x_2 , respectively.

If the MC-UPQC is lossless, the active power demand supplied by Feeder1 consists of two parts:

- 1) The active power demand of load in Feeder1;
- 2) The active power demand for sag and interruption compensation in Feeder2.

Thus, Feeder1 current (I_{s1}) can be found as

$$U_{t1}I_{s1} = U_{l1}I_{l1}\cos\phi_1 + U_{sf1}I_{l2}\cos\phi_2$$

$$(1-x_1)U_{t1}I_{s1} = U_{l1}I_{o1}\cos\phi_1 + x_2U_{l2}I_{o2}\cos\phi_2$$

$$(1-x_1)I_{s1} = I_{o1}\cos\phi_1 + x_2I_{o2}\cos\phi_2$$

$$I_{s1} = (I_{o1}\cos\phi_1 + x_2I_{o2}\cos\phi_2)/(1-x_1)$$

From Fig., the voltage injected by the series VSC in Feeder1 and thus the power rating of this converter (S_{VSC1}) can be calculated as

$$U_{sf1} = U_{t1}\tan\Theta = U_0(1-x_1)\tan\Theta$$

$$\begin{aligned} S_{VSC1} &= 3U_{sf1}I_{s1} \\ &= 3U_0(1-x_1)\tan\Theta \end{aligned}$$

he shunt VSC current is divided into two parts.

- 1) The first part (i.e., I_{c1}) compensates for the reactive component (and harmonic components) of Feeder1 current and can be calculated from Fig. as

$$\begin{aligned} I_{c1} &= (I_{l1}^2 + I_{s1}^2 - 2I_{l1}I_{s1}\cos(\phi_1 - \Theta))^{1/2} \\ &= (I_{o1}^2 + I_{s1}^2 - 2I_{o1}I_{s1}\cos(\phi_1 - \Theta))^{1/2} \end{aligned}$$

Where I_{s1} is calculated. This part of the shunt VSC current only exchanges reactive power (Q) with the system.

- 2) The second part provides the real power (P), which is needed for a sag or interruption compensation in Feeder2. Therefore, the power rating of the shunt VSC can be calculated as

$$\begin{aligned} S_{VSC2} &= 3U_{l1}I_{pf} = 3(Q^2 + P^2)^{1/2} \\ &= 3((U_{l1}I_{c1})^2 + (U_{sf1}I_{l2}\cos\phi_2)^2)^{1/2} \\ &= 3U_0(I_{c1}^2 + (x_2I_{o2}\cos\phi_2)^2)^{1/2} \end{aligned}$$

Where I_{c1} is calculated. Finally, the power rating of the series-VSC in Feeder2 can be calculated. For the worst-case scenario (i.e., interruption compensation), one must consider $x_2=1$. Therefore

$$S_{VSC3} = 3U_{sf2}I_{l2} = 3x_2U_0I_{o2}$$

4. Simulation Results

The proposed MC-UPQC and its control schemes have been tested through extensive case study simulations using PSCAD/EMTDC. In this section, simulation results are presented; and the performance of the proposed MC-UPQC system is shown.

4.1. Distortion and Sag/Swell on the Bus Voltage

Let us consider that the power system in Fig. 2 consists of two three-phase three-wire 380(v) (rms, L-L), 50-Hz utilities. The BUS1 voltage (u_{t1}) contains the seventh-order harmonic with a value of 22%, and the BUS2 voltage (u_{t2}) contains the fifth-order harmonic with a value of 35%. The BUS1 voltage contains 25% sag between $0.1s < t < 0.2s$ and 20% swell between $0.2s < t < 0.3s$. The BUS2 voltage contains 35% sag between $0.15s < t < 0.25s$ and 30% swell between $0.25s < t < 0.35s$. The nonlinear/sensitive load L1 is

a three-phase rectifier Load which supplies an RC load of 10Ω and $30F$. Finally, the critical load L2 contains a balanced RL load of 10Ω and $100mH$.

The MC-UPQC is switched on at $t=0.02$ s. The BUS1 voltage, the corresponding compensation voltage injected by VSC1, and finally load L1 voltage are shown in Fig.

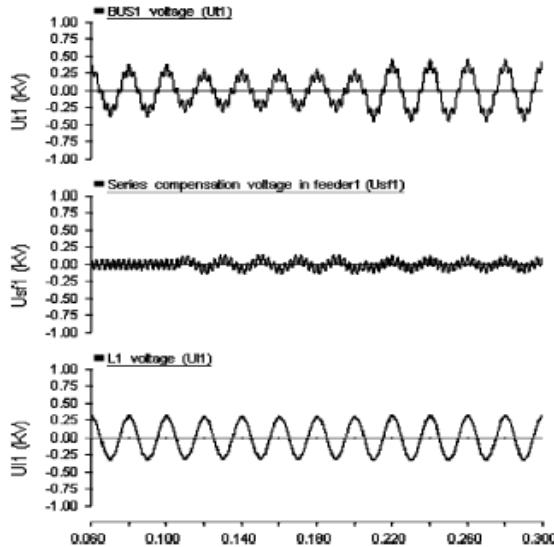


Fig 4.1 BUS1 voltage, series compensating voltage and load Voltage in Feeder1

In all figures, only the phase a waveform is shown for simplicity. Similarly, the BUS2 voltage, the corresponding compensation voltage injected by VSC3, and finally, the load L2 voltage are shown in Fig.

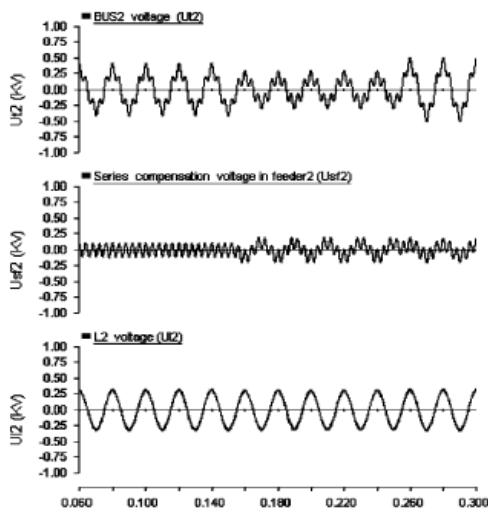


Fig 4.2 BUS2 voltage, series compensating voltage, and load Voltage in Feeder2.

As shown in these figures, distorted voltages of BUS1 and BUS2 are satisfactorily compensated for across the loads L1 and L2 with very good dynamic response. The nonlinear load current, its corresponding compensation current injected by VSC2, compensated Feeder1 current, and finally, the dc-link capacitor voltages are shown in Fig.

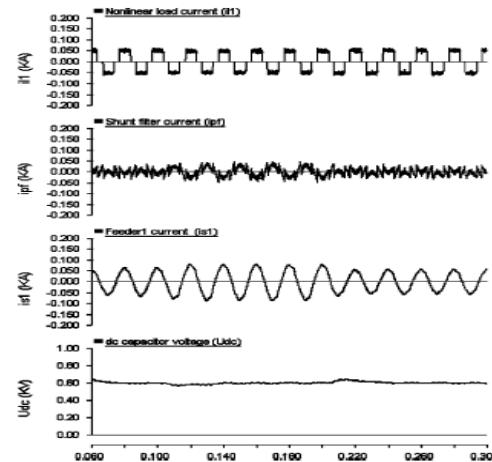


Fig 4.3 Nonlinear load current, compensating current, Feeder1 current and capacitor voltage

The distorted nonlinear load current is compensated very well, and the total harmonic distortion (THD) of the feeder current is reduced from 28.5% to less than 5%. Also, the dc voltage regulation loop has functioned properly under all disturbances, such as sag/swell in both feeders.

4.2. Upstream Fault on Feeder2

When a fault occurs in Feeder2 (in any form of L-G, L-L-G, and L-L-L-G faults), the voltage across the sensitive/critical load L2 is involved in sag/swell or interruption.

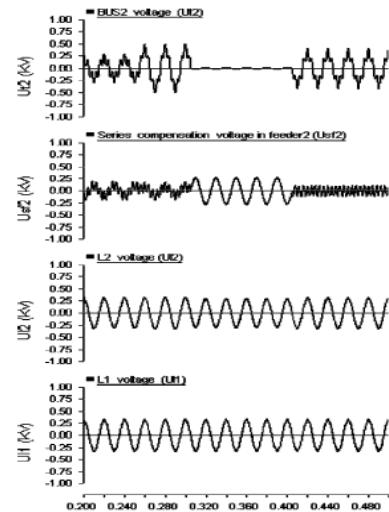


Fig 4.4 Simulation results for an upstream fault on Feeder2: BUS2 voltage, Compensating voltage, and loads L1 and L2 voltages.

This voltage imperfection can be compensated for by VSC2. In this case, the power required by load L2 is supplied through VSC2 and VSC3. This implies that the power semiconductor switches of VSC2 and VSC3 must be rated such that total power transfer is possible. This may increase the cost of the device, but the benefit that may be obtained can offset the expense. In the proposed

configuration, the sensitive/critical load on Feeder2 is fully protected against distortion, sag/swell, and interruption. Furthermore, the regulated voltage across the sensitive load on Feeder1 can supply several customers who are also protected against distortion, sag/swell, and momentary interruption. Therefore, the cost of the MC-UPQC must be balanced against the cost of interruption, based on reliability indices, such as the customer average interruption duration index (CAIDI) and customer average interruption frequency index (CAIFI). It is expected that the MC-UPQC cost can be recovered in a few years by charging higher tariffs for the protected lines. The performance of the MC-UPQC under a fault condition on Feeder2 is tested by applying a three-phase fault to ground on Feeder2 between $0.3s < t < 0.4$ s. Simulation results are shown in Fig.

4.3. Load Change

To evaluate the system behavior during a load change, the nonlinear load L1 is doubled by reducing its resistance to half at $t=0.5$ s. The other load, however, is kept unchanged. The system response is shown in Fig.

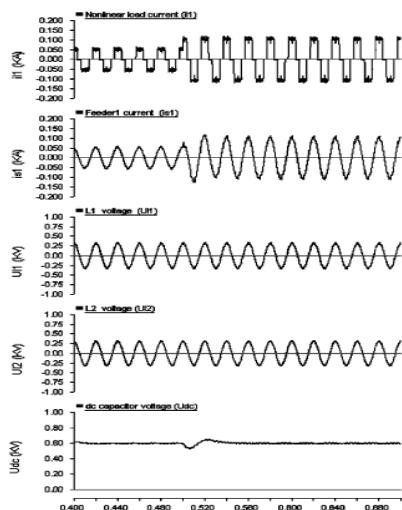


Fig 4.5 Simulation results for load change: nonlinear load current, Feeder1 current, load L1 voltage, load L2 voltage, and dc-link capacitor voltage.

It can be seen that as load L1 changes, the load voltages u_{l1} and u_{l2} remain undisturbed, the dc bus voltage is regulated, and the nonlinear load current is compensated.

4.4. Unbalance Voltage

The control strategies for shunt and series VSCs, which are introduced in Section II, are based on the d-q method. They are capable of compensating for the unbalanced source voltage and unbalanced load current. To evaluate the control system capability for unbalanced voltage compensation, a new simulation is performed. In this new simulation, the BUS2 voltage and the harmonic components of BUS1 voltage are similar to those given in Section IV. However, the fundamental component of the BUS1 voltage ($u_{t1,\text{fundamental}}$) is an unbalanced three-phase

voltage with an unbalance factor (u_-/u_+) of 40%. This unbalance voltage is given by

$$0.31\cos(\omega t+46^\circ)$$

$$U_{t1,\text{fundamental}} = 0.31\cos(\omega t-106^\circ)$$

$$0.155\cos(\omega t-210^\circ)$$

The simulation results for the three-phase BUS1 voltage series compensation voltage, and load voltage in feeder 1 are shown in Fig.

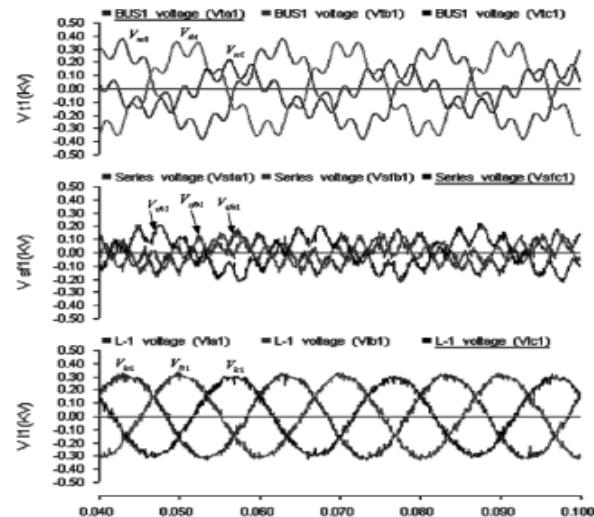


Fig 4.6 BUS1 voltage, series compensating voltage, and load voltage in Feeder1 Under unbalanced source voltage.

The simulation results show that the harmonic components and unbalance of BUS1 voltage are compensated for by injecting the proper series voltage. In this figure, the load voltage is a three-phase sinusoidal balance voltage with regulated amplitude.

Conclusion

In this paper, a new configuration for simultaneous compensation of voltage and current in adjacent feeders has been proposed. The new configuration is named multi-converter unified power-quality conditioner (MC-UPQC). Compared to a conventional UPQC, the proposed topology is capable of fully protecting critical and sensitive loads against distortions, sags/swell, and interruption in two-feeder systems. The idea can be theoretically extended to emultibus/MultiFinder systems by adding more series VSCs. The performance of the MC-UPQC is evaluated under various disturbances.

References

- Hamid Reza Mohammad (2009), Multiconvertor Unified Power Quality Conditioning System: MC-UPQC IEEE Transactions on Power Delivery.
- R.Rezaeipour (2008) Review of Novel control strategies for UPQC Internal Journal of Electric and power Engineering.
- M.V. Kasuni Perera (2007.) Control of a Dynamic Voltage Restorer to compensate single phase voltage sags Master of Science.

M. Basu, S. P. Das, and G. K. Dubey (2007), Comparative evaluation of two models of UPQC for suitable interface to enhance power quality, Elect. Power Syst.

A. K. Jindal, A. Ghosh, and A. Joshi (2007), Interline unified power quality conditioner, IEEE Trans. Power Del.

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