

## Research Article

## Power Factor Correction (Boost PFC Converter with Two-Switch Clamped Flyback Converter)

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### Abstract

The devices such as diode and thyristor are generally used in industrial, commercial and residential applications hence need to undergo rectification for their proper functioning and operation. They are connected to the grid comprising of non-linear loads and thus have non-linear input characteristics, which results in production of non-sinusoidal line current. Due to the increasing demand of these devices, the line current harmonics pose a major problem by degrading the power factor of the system thus affecting the performance of the devices. Hence there is a need to reduce the line current harmonics so as to improve the power factor of the system. This has led to designing of Power Factor Correction circuits. A single-stage AC/DC converter achieving power factor correction PFC, intermediate bus voltage regulation, and output voltage regulation is simulated and implemented in open loop. The converter is formed by a boost PFC converter with a two-switch clamped flyback converter into a single power stage circuit. The current stress of the main power switch is reduced due to separated conduction period of the two source currents flowing through the power switch. A dual-loop current mode controller is simulated to achieve PFC, and ensure independent bus voltage and output voltage regulations. This paper aims to achieve simulations results of 24-V/100-W in PSIM to confirm the theoretical analysis of the S2PFC converter

**Keywords:** PFC, S2PFC, Bus Voltage regulation, Output Voltage regulation, Dual Loop Current control mode, Psim.

### Introduction

Series connection of a power factor correction (PFC) circuit such as boost converter with an isolated dc/dc converter such as flyback and forward converters is a common practice to implement both power factor correction and fast output regulation of offline power supplies. In order to reduce the circuit and control system complexity and to lower the total cost that suitable for low power applications, single-stage power-factor-corrected S<sup>2</sup>PFC ac/dc converters have been introduced (Huang-Liahng Jou *et al*, April 2005). The two power stages of the PFC circuit and the dc/dc converter are simplified by sharing a common switch (or a pair of switches). By allowing the boost inductor to operate in discontinuous conduction mode (DCM), PFC and fast output voltage regulation can be performed simultaneously using a single-loop voltage feedback controller. Among S<sup>2</sup>PFC converters, the single-switch type S<sup>2</sup>PFC converter is found low cost and compact. However, the voltage spike caused by the leakage energy of transformer has to be dealt with to protect the switch from exceeding the maximum tolerable voltage and to reduce switching loss. To overcome this problem, various passive and active snubber circuits are proposed to suppress the voltage stress on the switch and to dissipate or recycle the leakage energy the snubber stored. Two-transistor clamped

isolated converters are useful in clamping the switch stresses to the input voltage as well as recycling the leakage energy back to the source. S<sup>2</sup>PFC converter which a boost converter into a two-transistor clamped flyback converter and shared the same switch S<sub>1</sub> based on S<sup>2</sup>PFC concept in (Huang-Liahng Jou *et al*, April 2005). Switch S<sub>1</sub> and S<sub>2</sub> are synchronized in action so that when they are turned on, the inductors L<sub>1</sub> and L<sub>m</sub> are both charged up linearly by input voltage v<sub>in</sub> and storage capacitor C<sub>B</sub>, respectively. When the switches turn off, the energy stored in L<sub>1</sub> and L<sub>m</sub> is transferred to the storage capacitor and the load, respectively. The leakage energy is transferred back to the storage capacitor, and the switches are clamped to the intermediate bus voltage V<sub>B</sub>.

Owing to the input–output voltage characteristic of the boost converter, the intermediate bus voltage is always higher than the peak input voltage. For universal line input applications (i.e., 100–230V) this voltage usually exceeds 450V at high line input condition, resulting in high-voltage stress on semiconductor devices such as power transistors and diodes. It has been shown that the intermediate bus voltage of the S<sup>2</sup>PFC converter where the dc/dc stage working in continuous conduction mode (CCM) is inversely proportional to the load current (S. Luo. *et al*, 1999) This voltage may even rise up higher (e.g., 1000V) at high line light load condition. It is more expensive for higher voltage rating capacitor.

To suppress the voltage stress across the storage capacitor, various approaches are introduced to reduce the

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energy feeding the storage capacitor. Variable switching frequency (VSF) (M.H.L. Chow *et al*, January 2000) limits the input power pumped to the storage capacitor by increasing the switching frequency at decreasing load. However, large load variation results in wide variation range in switching frequency. Even with ten times of switching frequency range, the storage capacitor voltage is hardly suppressed to below 450V. The optimization of filtering is yet another issue when using VSF to cope with the high-voltage stress problem. Bulk capacitor voltage feedback can effectively reduce the voltage stress by curtailing the charging current in the boost inductor when the load is decreasing. However, a dead angle of input current occurs when the line input voltage is lower than the feedback voltage, resulting in poor power factor. By adding a parallel PFC converter with the diode-capacitor filter, the bus voltage is clamped at the peak input voltage and input current can design to comply with IEC 61000-3-2 requirement. However, the bus voltage still varies with the input voltage. Therefore, the capacitance has to be large enough for low-line operation. Operating both stages in DCM may reduce the voltage stress but it may not favor high output current/power applications. Direct power transfer is introduced to place an auxiliary coupled winding in series with the charging path of boost inductor, "stealing" energy to output directly after the first power process. The voltage stress is reduced rapidly while maintaining high power factor. Conversion efficiency is also improved, but the bus voltage in all of these methods still varies largely when input line voltage varies (Dylan Dah-Chuan Lu *et al*, January 2008).

Problem in  $S^2PFC$  converter is the extra current stress on the switch (or a pair of switches) when compared with the two-stage approach because it has to handle all the input currents from the line input voltage and the bus voltage simultaneously. Conduction and switching losses are therefore increased which deteriorate the conversion efficiency. Besides reduction of voltage stress on storage capacitor, the bulk capacitor voltage feedback is found useful in reducing the switch current stress, but the reduction of current stress also causes an increase in input current harmonics. Recently, load current feedback technique is introduced in which the load information is brought forward to the input stage, controlling the input current directly. And at any time the switch handles current from one voltage source, either the line input voltage or the storage capacitor. However, the high input current harmonics problem still exists. The authors in and attempted to control the bus voltage and output voltage in  $S^2PFC$  converters but due to the integrated structure, the currents from both input sources (ac mains and storage capacitor) cannot be separated. Hence, the current stress issue remains. Moreover, since the duty cycle varies largely for universal input applications, an extra range switch is needed (Dylan Dah-Chuan Lu *et al*, January 2008).

### Principle of operation

#### Circuit Description

The boost-flyback  $S^2PFC$  converter is shown in Figure 1 (J. Arrillaga *et al*, 1985). It consists of an input inductor

$L_I$ , a two-transistor ( $S1$  and  $S2$ ) clamped flyback converter with transformer  $T1$  and a storage capacitor  $C_B$ . Inductor  $L_I$  is used to shape the input current for PFC function and to feed  $C_B$ . Transformer  $T1$  with turn ratio  $N$  is used to store energy from  $C_B$  and couple the energy stored in the magnetizing inductance  $L_m$  to output load at transistor turnoff period. Storage capacitor  $C_B$  serves as a storage element for absorption of power imbalance between input and output powers as well as maintains output voltage constant. Diodes  $D_1$  and  $D_2$  are used to recycle the leakage energy in  $T1$  back to  $C_B$  and to clamp the drain-to-source voltages of switch  $S2$  and  $S1$  to bus voltage  $V_B$  simultaneously.  $D_3$  is a bypass diode for charging of  $C_B$  to provide necessary housekeeping power at startup. Once  $V_B$  rises and becomes higher than input voltage,  $D_3$  is reversed biased.

#### Circuit Operation

To simplify the analysis of operation, it is assumed that all semiconductor devices are ideal. The capacitances of  $C_B$  and  $C_o$  are so large that the ripple voltage on them is negligible;  $V_B$  and  $V_o$  are constant dc voltage sources. The rectified input voltage  $|v_{in}|$  is essentially constant within each switching cycle as the switching frequency  $f_s (=1/T_s)$  is much higher than the line frequency. Finally, the boost inductor  $L_I$  works in DCM, whereas the primary inductance of flyback transformer  $L_m$  operates in CCM.

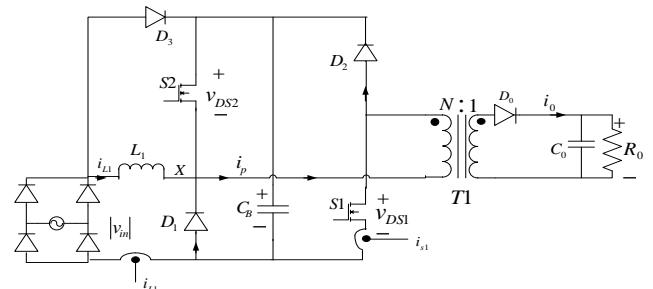


Figure 1: Boost Flyback  $S^2PFC$

**Mode 1( $T_0 - T_1$ ):** Both the switches  $S1$  and  $S2$  are closed. As the intermediate bus voltage  $V_B$  is higher than the rectified input voltage  $|v_{in}|$  at all times, the bridge diodes are reverse biased. Therefore, inductor  $L_I$  is not charging and  $i_{L_I}$  is zero. Capacitor  $C_B$  is discharged through  $S2-L_m-S1$ , as shown in the equivalent circuit in Figure 2 [Dylan Dah-Chuan Lu *et al*, January 2008].

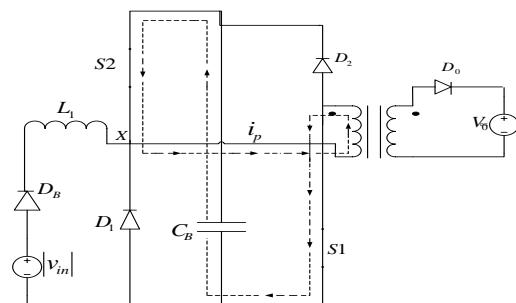


Figure 2: Mode 1( $T_0 - T_1$ )

The principle of operation of boost-flyback  $S^2PFC$  converter is illustrated from below. The key theoretic waveforms within two switching cycles are shown in Figure 7. The four modes of operation in steady state are explained below. Note that the input voltage and bridge rectifier have been modeled as a voltage source in series with a diode  $D_B$ . Before the time  $t=T_0$ , switches  $S1$  and  $S2$  are turned off and no current is flowing in the primary side (i.e.,  $i_{L1} = i_p = i_{D1} = i_{D2} = 0$ ). Meanwhile, diode  $D_0$  is in conduction state and transformer  $T1$  continues delivering energy to output  $V_0$  through current  $i_{D0}$ .

Energy is being stored in the flyback transformer  $T1$ , and the current  $i_p$  increases linearly with a slope. A blocking voltage equal to  $V_B/N + V_0$  is applied across output diode  $D_0$ , and  $D_0$  is reversed biased. The output voltage  $V_0$  is sustained by  $C_0$ . Note that only one voltage source (i.e.,  $C_B$ ) provides the current of two switches, which equals  $i_p(t - T_0)$ .

$$\frac{di_p}{dt} = \frac{V_B}{L_m} \quad (1)$$

**Mode 2( $T_1 - T_2$ ):** Mode 2 is initiated by turning off  $S2$  while  $S1$  remains in on-state. The parallel capacitance of  $S2$  is charged up so that the drain-to-source voltage of  $S2$ ,  $v_{DS2}$ , rises towards  $V_B$  until it is clamped by  $V_B$ , as shown in Figure 3. During this period, the energy stored in  $T1$  cannot be coupled to output as  $S1$  is still closed. Because  $i_p$  cannot sustain a sudden change of current direction,  $D_1$  is turned on to maintain the current flow in  $T1$ . The voltage applied across primary winding of  $T1$  is thus zero (assume  $D_1$  has zero forward voltage drop). Namely,  $T1$  is free-wheeling within this interval and the rate of change of  $i_p$  is zero. Meanwhile, the rectified input voltage is applied on  $L_1$  and  $L_1$  is charged up linearly with a slope

$$\frac{di_{L1}}{dt} = \frac{|V_{in}|}{L_1} \quad (2)$$

By the KCL, the current into node  $X$  (as shown in Figure 3) equals the current out of the node, we have the following relationship:

$$i_{L1} + i_{D1} = i_p \quad (3)$$

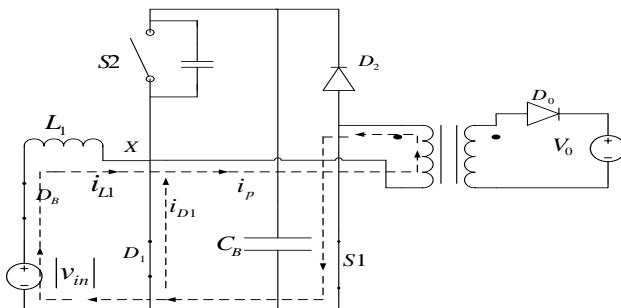


Figure 3: Mode 2( $T_1-T_2$ )

Therefore, the current in  $D_1$  is not a constant but is decreasing with the expression given by

$$i_{D1} = i_p(T_1) - \frac{|V_{in}|}{L_1}(t - T_1) \quad (4)$$

Where,  $i_p(T_1)$  is the peak of  $i_p$  at time equals  $T_1$ . It should be noted that the current of power switch  $S1$  during this mode equals  $i_p$  and is clamped at  $i_p(T_1)$  without increasing current stress even  $i_{L1}$  is charging up. In some cases, the inductor current may exceed the  $i_{p,pk}$ , diode  $D_1$  stops conducting,  $L_1$  and  $L_m$  are in series and charging up together. As  $L_m \gg L_1$ , the charging rate is small and so is the current stress on the switch, as shown in Figure 7.

**Mode 3( $T_2 - T_3$ ):** Mode 3 is begun when  $S1$  is also turned off. The parallel capacitance of  $S1$  is charged by  $i_p$ . The drain-to-source voltage of  $S1$ ,  $v_{DS1}$ , rises towards  $V_B$ , as shown in Figure 4. When  $v_{DS1}$  raises slight above  $V_B$ ,  $D_2$  is forward biased.  $v_{DS1}$  is clamped at  $V_B$ , and  $v_{DS2}$  is reduced to  $NV_0$ . Once again, inductor current  $i_{L1}$  cannot sustain a sudden change of current direction;  $D_2$  provides the path to maintain the current of  $L_1$ . When  $v_{DS1}$  raises slight above  $V_B$ ,  $D_2$  is forward biased.  $v_{DS1}$  is clamped at  $V_B$ , and  $v_{DS2}$  is reduced to  $NV_0$ .

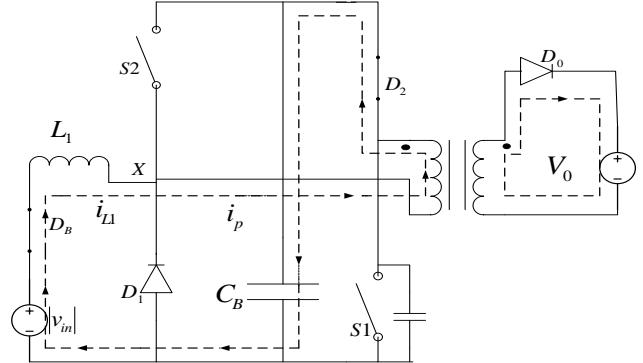


Figure 4: Mode 3( $T_2 - T_3$ )

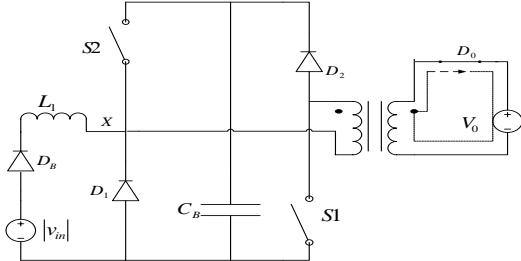
When  $v_{DS1}$  raises slight above  $V_B$ ,  $D_2$  is forward biased.  $v_{DS1}$  is clamped at  $V_B$ , and  $v_{DS2}$  is reduced to  $NV_0$ . Once again, inductor current  $i_{L1}$  cannot sustain a sudden change of current direction;  $D_2$  provides the path to maintain the current of  $L_1$ . The stored energy in  $L_1$  is being transferred to  $C_B$  through  $L_m$  and  $D_2$  with a down slope equals

$$\frac{di_{L1}}{dt} = \frac{V_B - |V_{in}| - NV_0}{L_1} \quad (5)$$

As point  $X$  reaches  $V_B - NV_0$ , a blocking voltage is set up on  $D_1$  and  $D_1$  is reverse biased. As the dotted end of  $T1$  is positive with respect to the non-dotted ends and voltage across primary side rises and becomes slightly over  $NV_0$ ,  $D_0$  is forward biased, and the energy stored in  $T1$  is transferred to the load.  $i_{D0}$  Conducts with a rate of change of current equals

$$\frac{di_{D0}}{dt} = \frac{N(V_B - |V_{in}| - NV_0)}{L_1} - \frac{N^2 V_0}{L_m} \quad (6)$$

**Mode 4( $T_3 - T_4$ ):** This mode is started when  $i_{L1}$  has decreased to zero. Note that Mode 4 must exist, otherwise the transfer of energy stored in  $L_1$  to  $C_B$  has not yet completed and  $i_{L1}$  will enter in CCM. A sudden rise in  $i_{L1}$  would occur that causes high input current harmonics distortion. Transformer  $T1$  continues to deliver the rest of energy to output through  $D_0$ , as shown in Figure 5.



**Figure 5:** Mode 4(T3-T<sub>4</sub>)

The rate of change of current in  $D_0$  is negative and equals

$$\frac{di_{D0}}{dt} = \frac{N^2 V_0}{L_m} \quad (7)$$

After some time,  $S1$  and  $S2$  turns on again to begin the next switching cycle, the operation described above will repeat (Dylan Dah-Chuan Lu et al, January 2008).

### Control of S<sup>2</sup>PFC Converter

The main objective of the control system is to find a simple and effective way to control the two switches  $S1$  and  $S2$  so that *PFC* is achieved, the bus voltage  $V_B$  and the output voltage  $V_o$  are regulated as line and load vary.

#### Power Factor Correction

Given that the input voltage is a rectified sinusoidal wave, i.e.,  $|v_{in}| = V_m |\sin(wt)|$ , where  $w$  and  $V_m$  are the angular frequency and the peak value of line input voltage. Assume the inductor works in *DCM*, the instantaneous input current is obtained by averaging the inductor current over a switching period, which is given by

$$\bar{i}_{L1}(t) = \frac{d_3^2 T_s V_m}{2 L_1} |\sin(wt)| \left( \frac{1}{1 - F(wt)} \right) \quad (8)$$

Where,

$$F(wt) = \frac{V_m |\sin(wt)|}{V_B - N V_o} \quad (9)$$

As long as  $L_1$  works in *DCM* throughout the line cycle,  $i_{L1}$  flows into the converter for every switching period (i.e., in Mode 2) and duty cycle  $d_3$  keeps relatively constant, *PFC* is achieved automatically because  $L_1$  functions as a boost inductor. At Mode 2, when  $S2$  is turned off and  $S1$  remains on, the input current flows into the converter and charges  $L_1$  linearly. As seen from (2), as soon as input voltage  $|v_{in}|$  increases from zero, there is always input current flowing through  $L_1$ .

In order to obtain good power factor of the converter, all the parameters in (8), should be kept relatively constant, except for the sine term which changes according to input line voltage. The bus voltage  $V_B$  contains twice the line frequency voltage ripple because it serves as a buffer to balance the difference of input and output powers. The control loop of *PFC* should have a cutoff frequency far behind the line frequency to avoid input current distortion, and therefore its response is slower than that of the *dc/dc* counterpart. This implies duty cycle  $d_3$  is relatively

constant throughout the line half period (Dylan Dah-Chuan Lu et al, January 2008).

The converter operates in fixed frequency; the nonlinear factor would be the function  $F(wt)$  which will cause input current distortion. From (9), it shows that the higher the bus voltage  $V_B$  and the smaller turn ratio  $N$  and the output voltage  $V_o$ , the smaller  $F(wt)$  will be (Dylan Dah-Chuan Lu et al, January 2008).

#### Bus Voltage Regulation

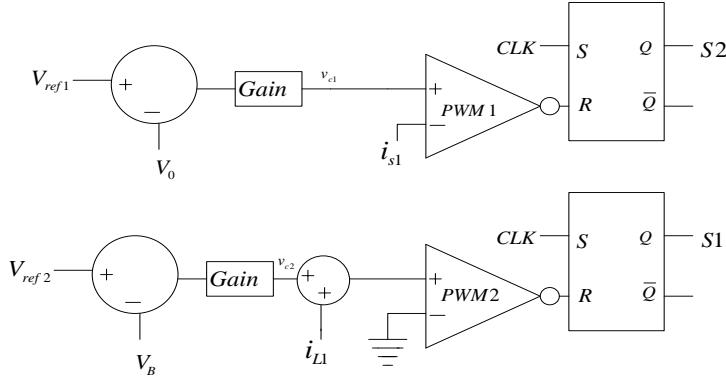
At startup, the bus voltage is essentially zero, though a residual charge may exist. When input voltage applies across the converter input terminals, the storage capacitor  $C_B$  is charged up via  $D_3$ . The presence of  $D_3$  also prevents the inductor from saturation at startup. The bus voltage rises to the peak value of input voltage. The converter begins to deliver energy to  $C_B$  through  $L_1$ , and  $V_B$  rises gradually to the designed reference value. The bus voltage is sensed and regulated by controlling the duration of energy stored in  $L_1$  during Mode 2. At Mode 3, energy stored in  $L_1$  will be delivered to  $C_B$ . Therefore, Modes 2 and 3 are dedicated for *PFC* and bus voltage regulation.

#### Output Voltage Regulation

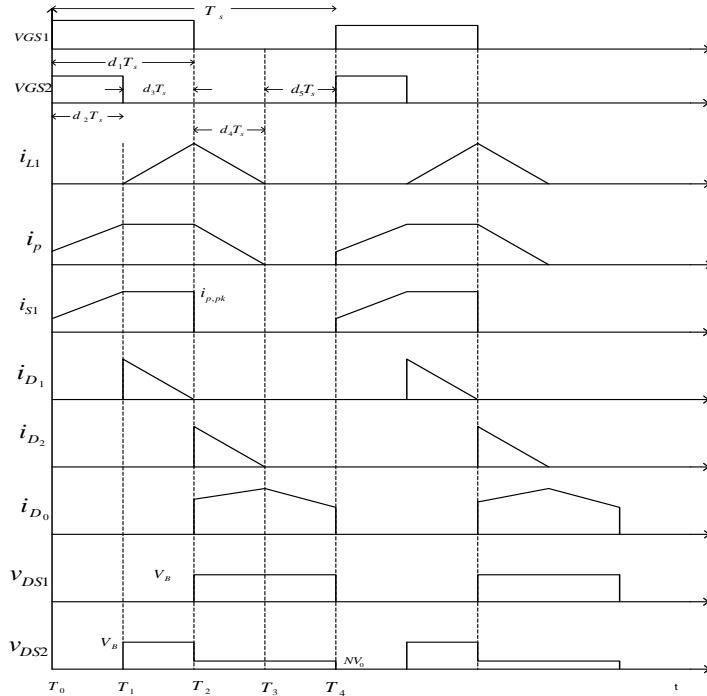
The bus voltage is used to provide regulation of output voltage  $V_o$ . This happens during Mode 1, when both switches  $S1$  and  $S2$  are turned on. At mean to full load, transformer  $T1$  is working in *CCM* even if there exists large load current variation; the change of duty cycle in this mode is slight. It is due to the negative current feedback that the transformer regulates its primary current according to the demand of secondary current. As seen from (7), the rate of change of output diode current is proportional to the output voltage  $V_o$ . For example, if a decrease of load (or increase of load resistance  $R_o$ ) occurs, the instantaneous output current is constant and causes  $V_o$  to increase. This steepens the down slope of output diode current. The primary transformer current will be decreased so less current is drawn from  $C_B$ . When the load becomes light,  $T1$  may work in *DCM*. The duty cycle can vary freely in this mode to keep output constant as there is no other current path. Therefore, Mode 1 is dedicated for output voltage regulation.

#### Current Mode Control

Even though voltage mode control is the simplest way to achieve control purposes, current mode control monitors circuit currents to provide fast response and protection from abnormal operations such as over-current. Peak current mode control can be achieved easily on the *dc/dc* part by sensing the current of switch  $S1$  directly using current sensor which is placed in series with  $S1$ , as shown in Figure 1. The *PFC* part is implemented also using peak current mode control. One of the direct methods to sense the inductor (or input) current is by placing a current sensor in the return path, as shown in Figure 1. Although the *PFC* operates with constant duty cycle  $d_3$  and peak current limit, the average inductor current indeed changes



**Figure 6:** Configuration of dual-loop current mode PWM control for Simulation



**Figure 7:** Switching waveforms of the S2PFC converter during two switching period

proportionally with input voltage to shape input current, as seen from (5). For example, when  $|v_{in}|$  increases, the rate of change of  $i_{L1}$  decreases and the discharge period  $d_4T_s$  extends as input voltage is in series with the current path, more current flows into the converter and  $\dot{i}_{L1}$  increase as a result.

The controls on  $V_0$  and  $V_B$  on are independent due to the circuit configuration that allows independent power processing stages and independent currents paths for monitoring and regulating of  $V_0$  and  $V_B$ . It can be seen from Figure 7 that during Mode 1, only flyback  $dc/dc$  part is working. No current from line input flows into the circuit. The current through current sensor1 equals the bus capacitor discharging current. During Mode 2, flyback transformer current is constant while boost inductor current  $i_{L1}$  builds up. The current through current sensor 2 is  $i_{L1}$  only (J. Arrillaga *et al*, 1985).

#### Control Realization

Figure 6 shows the simplified schematic blocks of the dual loop current mode control for the converter. Both loops

are triggered by the same clock to have synchronized ON pulse. When a clock pulse is generated, both  $S1$  and  $S2$  go to high state. At startup,  $C_B$  is charged up and able to couple energy to output through  $T1$ . The first loop is used for output voltage regulation. The output voltage is sensed and subtract with  $ref1$  than multiply with gain and an error control voltage  $v_{cl}$  is generated.  $v_{cl}$  is compared to the switch current of  $S1$  by comparator  $PWM\ 1$  to produce desired off duty cycle for  $S2$  through the  $SR$ -type flip-flop. The second loop is used for  $PFC$  and bus voltage regulation. The bus voltage is sensed and subtract with  $ref2$  than multiply with gain and an error control voltage  $v_{c2}$  is generated.  $v_{c2}$  is summed with the inductor  $L_1$  current and compared to ground by comparator  $PWM\ 2$  to produce desired off-duty cycle for  $S1$  through the  $SR$ -type flip-flop (J. Arrillaga *et al*, 1985).

#### Experimental Results

The simulation result has been carried out for the  $S^2PFC$  converter shown in Figure 1. The converter has 24V/100W

output with bus voltage of 400V. The operation switching frequency is at 50 kHz. Peak current mode is control strategy both for boost and flyback parts. The result shows that the bus voltage and output voltage gets regulated. The input current also maintains the sinusoidal wave shape. The circuit parameter for simulations that has been used here are as follows. The bus voltage is tightly regulated at 400V throughout entire line and load conditions due to the integrated but independent converter structure and control which make the simultaneous control of bus and output voltages possible.

**Table 1:** Component Parameters

#### Circuit Parameters of $S^2$ PFC Converter

Sr. No.	Quantity	Value
1	Source Voltage $V_s$	100V
2	Inductor $L_I$	$26.5\mu H$
3	Bus Capacitor $C_B$	$470\mu F$
4	Magnetizing Inductance $L_m$	$3.05mH$
5	Output Capacitor $C_o$	2mF
6	Output Resistance $R_o$	$5.76\Omega$
7	Number of Turns Ratio $N$	2.5
8	Filter Capacitor $C_f$	$0.15\mu F$

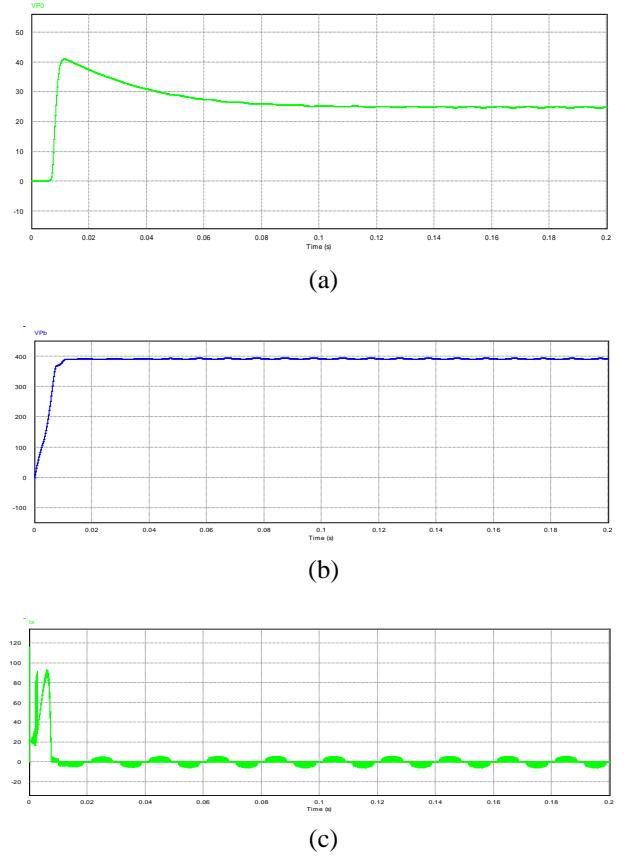
#### Simulation of $S^2$ PFC Converter in Open Loop Control

Figure 8 shows the output voltage, bus voltage and supply current at 100 V input voltage. Output voltage and bus voltage are regulated as per design value. Figure 8 (c) shows the supply current which is near to sinusoidal but very high ripple in the supply current because filter is not connected at AC side, and power factor is 0.764 from the open loop simulation. Figure 9 shows the switching waveform of the converter. We can observe that there appears negative inductor current because when both  $S_1$  and  $S_2$  are turned on,  $C_B$  will momentarily charge up the input filter capacitor, which is located in between the bridge rectifier and inductor, and is for EMI reduction purposes. The inductor current then experiences a short duration of reverse polarity. It can be seen that when both the switches are in turn OFF position then the diode  $D_0$  starts conducting.

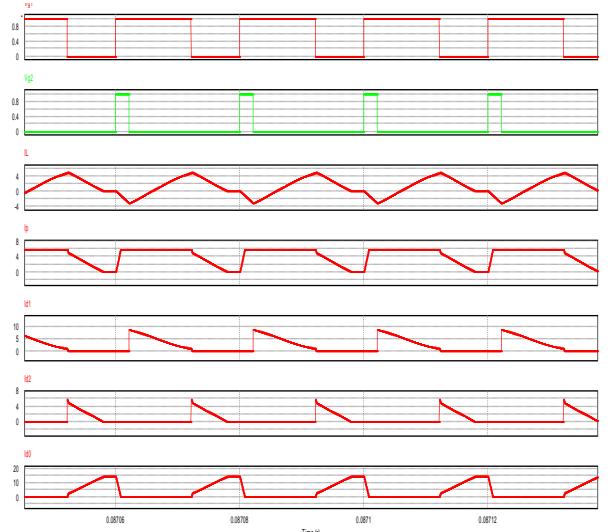
#### Simulation of $S^2$ PFC Converter in Closed Loop Control

Figure 10 shows the waveforms of the converter when both switches are controlled by closed loop control. The Figure 10 show the output results for input voltage of 100 V. Waveform shown in Figure 10 is got when a bus capacitor is initially charge at its reference value. As shown simulation results Show the output voltage is less than design value but it is regulated, bus voltage is also regulated, supply current is pure sinusoidal, and power factor is 0.99 from the simulation.

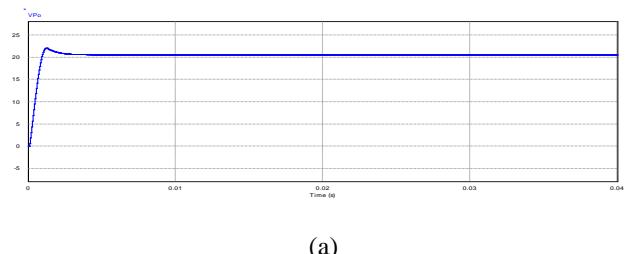
#### Simulation Results

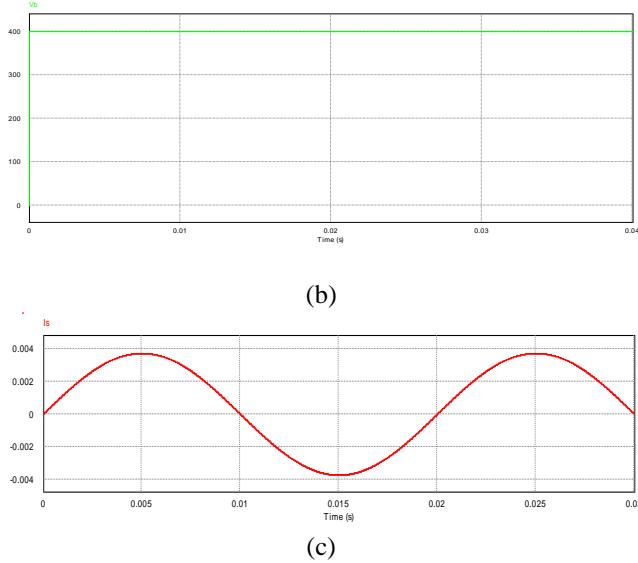


**Figure 8:** Simulated waveform of  $S^2$ PFC converter in open loop control (a) Output voltage (b) Bus voltage (c) Supply current



**Figure 9:** Simulated waveforms of  $S^2$ PFC Converter in open loop control during switching period





**Figure 10:** Simulated waveform of  $S^2$ PFC converter in closed loop control (a) Output voltage (b) Bus voltage (c) Supply current

## Conclusion

The simulation of the topology (Dylan Dah-Chuan Lu *et al*, January 2008) has been implemented to prove the theoretical analysis. Here we can conclude that the theoretical and the simulation analysis give us a clear idea that the bus voltage and output voltage are very well regulated. From the waveform of the input current we can see that the current is purely sinusoidal when control is applied to the topology. Hence there is a correction in power-factor that comes at about 0.99 when control loop is applied.

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