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Research Article

# Study of Electrical Characteristics of SOI n-MOSFET at Various Technological Nodes

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***Abstract***

*The current interest is focused principally on the low voltage and low power digital CMOS usage requiring deep submicron devices. For deep submicron devices Silicon on Insulator (SOI) MOSFETS are better to their counterparts using bulk CMOS. There is a concern about the aptness of SOI for various electrical parameters especially in the submicron domain. This paper Weigh the performance of SOI at different technological nodes. The focus of our paper is on leakage current, threshold voltage and subthreshold conduction of SOI fabrication in the submicrometer scope. We have fabricated soi n-MOSFET using Silvaco-Athena and carried out simulations for leakage current, threshold voltage and subthreshold conduction at 1micron, 91nm and 64nm of technological nodes. Silvaco-Athena design and simulation results using Atlas are presented, that shows soi technology is still better in the submicron region. Kink effect analysis is also carried out.*

***Keywords:*** *MOSFET, SILVACO-ATHENA, ATLAS, SOI, Subthreshold Conduction, Submicron Technology*

## 1. Introduction

SOI (Silicon-on-Insulator) CMOS technology is suitable another current important technology for VLSI. By reason inheritable features, SOI CMOS technology is particularly capable of providing deep-submicron VLSI devices for next generation high-speed, low-power, system applications using a low-power supply voltage. Thanks to advance in processing technology, SOI CMOS technology has been used to improvement multi-giga-bit DRAM, 1 GHz microprocessors, and other high-speed low-power computer-related VLSI circuits. By reason much smaller parasitic capacitances, SOI CMOS devices have also been used to integrate high-speed low-power VLSI circuits.
Presently, the requirement on low-voltage VLSI circuit designs using deep-submicron SOI CMOS technology have proceed dramatically. After these days the development of the supporting environment for possibility the demands on the development of the SOI CMOS IC designs for VLSI system experiment is not paced accordingly. The microelectronics manufacture is interested in becoming popular with the SOI CMOS device behaviors and wants to know the performance of SOI in deep submicron scope. Multiplicity of unexpected parasitic elements can be formed by the figure. The paper provides brief inspection of SOI technology, section II deals with the different electrical parameters under consideration, section III presents the simulation results and discussion. The cross section of SOI collate to bulk is as shown in fig 1. SOI figure do not vary much from normal bulk CMOS. The major dispute is the insertion of the insulation layer beneath the devices. pacification of bottom junctions lowers parasitic capacitance and makes faster switching and/or lower power invisibility. The full discard in SOI provide no latch-up, denser layout, lower intervention between the analog and digital parts, lower losses in the passive components at high frequency, lower leakage current, enabling manipulation at higher temperature (250°C), thin active area and lower sensibility to radiations.

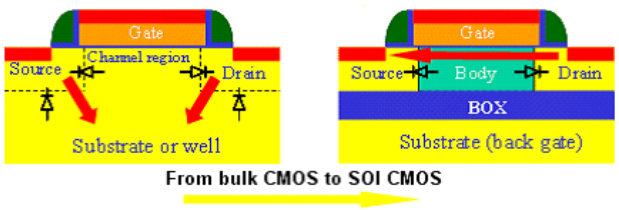


**Fig. 1** Migration from Bulk to SOI Structure

## 2. Electrical Properties of the SOI MOSFET

Demeanors of SOI CMOS devices are quite different from those of the bulk ones. Understanding the unique conduct of the SOI CMOS devices is important for designing SOI CMOS VLSI circuits.

### *A. Threshold Voltage and Leakage Current*

Procedure mutable alters the ratio of forward and reverse diode leakages, which will install new balanced voltages.

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Lower channels will also produce more impact ionization, resulting in more history effect. Conducting Hot Electron generation also simultaneously presents as Demission in device current. This Demission's dependence on channel length, and hence the electron-hole pair generation for a typical manufacture CMOS technology. Lower channels also produce bodies with less total volume. Smaller bodies contain less charge, and the decreased volume reduces the time necessary to obtain large excursions in body potential. Voltage of the supply affects confluence leakage, and will affect the body potential. Of weightage is not only the magnitude of forward and reverse leakage currents, but changes in the ratio of forward bias current to reverse bias current. Temperature strongly affects junction leakage and device threshold voltage, as well. less threshold voltage at higher temperatures increases the portion of the electron energy distribution capable of ionizing silicon lattice points. This afresh affects the potential where the current into the body is balanced with the current out of the body. Temperature also affects the leakages of the junctions themselves, straight affecting body charge content. The most main electrical property of the PD-SOI device is the History Effect. I-V characteristics of the MOSFET built in PD-SOI are no longer constant, but dependant on the amount of charge contained in the body of the device at any given time. The charge content of the body and the delivery of that charge caused by gate, source, and drain potentials determine the behavior of the device. Charge in the body is directly related to the potential of the body. The dependency of MOSFET threshold voltage on substrate bias is well known. Conceptually, body bias's effect on threshold voltage may be explained by how stringently this potential reverse-bias the junctions, which must be overcome by gate drive. The magnitude of charge included in the body is dependent on a number of factors which include: *Previous state of transistor, Schematic position of transistor {possible source, drain voltage ranges}, Slew rate of input, and load capacitance, Channel length and processing corner, Operating supply voltage, Junction temperature, Operating frequency and specific switch facto.*

*B. Subthreshold Analysis*

The Subthreshold behavior of an SOI MOS device depends on the thickness of the silicon thin-film, the doping solidity of the silicon thin-film, and the channel length. When the silicon thin-film is thick, partially depleted, the subthreshold slope of the SOI n-MOSFET device is identical to that of the bulk devices. While the silicon thin-film is thin, fully depleted, its subthreshold slope is much better with its value close to the ideal case due to the buried oxide isolation between the channel and the grounded substrate. In the case of a partially depleted device, a higher silicon thin film doping density leads to a worse inverse subthreshold slope silima to the bulk device. A hump in the subthreshold features can be bessen in mesa isolated SOI n-MOSFETs. The hunk is caused by the 2D effect, which results in a smaller threshold voltage for the sidewall channel as compared to the center channel.

*C. Kink Effect*

PD-SOI MOSFET transitions from collection into inversion and saturation, it moves through an interval of gate drive in the *conducting mode* where impact ionization peaks, generally at VDD/2. The injection of positive charge into the body has a noteworthy effect on the dynamic behavior of the device. Since a large sudden increase of positive charge will reduce threshold voltage, a *kink,* or increase in IDS may be observed when the gate voltage reaches approximately

VDD/2. This change in slope, observed at normal operating voltages, is often indicated to as the First Kink. A second kink, not nearly as noticeable as the first kink occurs after the first kink. As the device current increases, the body-to-source diodes can eventually forward-bias, enabling the flow of bipolar current in the figure. This bipolar device, in parallel with the intended MOSFET, tends to increase the MOSFET. For most usual applications, this second kink is usually overlooked. A third kink, of sorts, may be observed when the device is conducted at elevated voltages, as habitual during reliability stress testing. As the supply voltage increases, the kink just stated first appears at lower and lower gate voltages; at a sufficiently high VDD, impact ionization in the device's *nonconducting mode,* with the gate voltage at GND, causes positive charge to accumulate in the NFET body, disappointing threshold voltage before the gate is even turned on. The second kink is a concern as stressing parts at elevated voltage and temperature, when functionality is still required. The naturally lower threshold voltages caused by elevated stress temperatures exaggerates this impact ionization, further threatening circuit functionality. hence kink become because of impact ionization which charges the body of the device and raises body bias. It follows, then, that the more time the gate potential spends in the device region of performance which maximizes impact ionization, the much noticeable the kink will be i.e. the amount of kink would be expected to vary with gate switching frequency.

## 3. Simulation tools and Methodology Description

*3.1 Athena Inputs and Outputs*

Athena framework integrates several process simulation modules within a user-friendly environment provided by Silvaco TCAD interactive tools.


**Fig.2** Athena Input and Output Block diagram

Athena has evolved from a world-renowned Stanford

University simulator SUPREM-IV, with many new capabilities developed in collaboration with dozens of academic and industrial partners. Athena provides a convenient platform for simulating processes used in semiconductor industry: ion implantation, diffusion, oxidation, physical etching and deposition, lithography, stress formation and solicitation.

*3.2 Atlas Inputs and Outputs*

Within the device for a single bias ATLAS produces three types of output. The run-time output provides a guide to the progress of simulations running, and is where error messages and warning messages appear. Log files store all terminal voltages and currents from the device analysis, and solution files store two- and three dimensional data relating to the values of solution variables point.

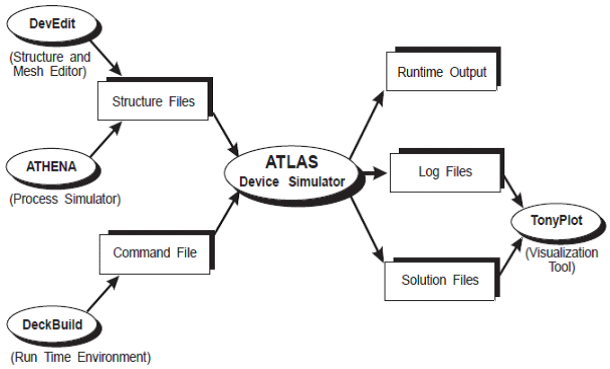


**Fig.3** Atlas Input and Output Block diagram

**4. Result and Discussion**

The SOI n-MOSFET is constructed using Silvaco Athena at various other technologies e.g. 65nm, 90nm, 1um and 3µm. The developed device consists of thin gate oxide. The device structure of SOI n-MOSFET at 1µm is as shown in fig.2.

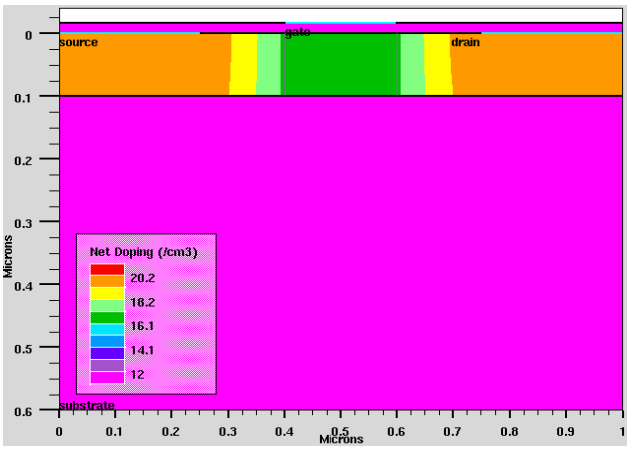


**Fig. 4.** SOI Device Structure of MOSFET at 1micron

The plots for the leakage current of SOI n-MOSFET at 1µm, 91nm and 64nm is as shown in fig. 5, fig. 6 and fig 7. The leakage current of corresponding default CMOS model from Silvaco-Athena is found to be much more than SOI models. When SOI models are compared for different device sizes then leakage current increases as the device size shrinks as indicated by table.

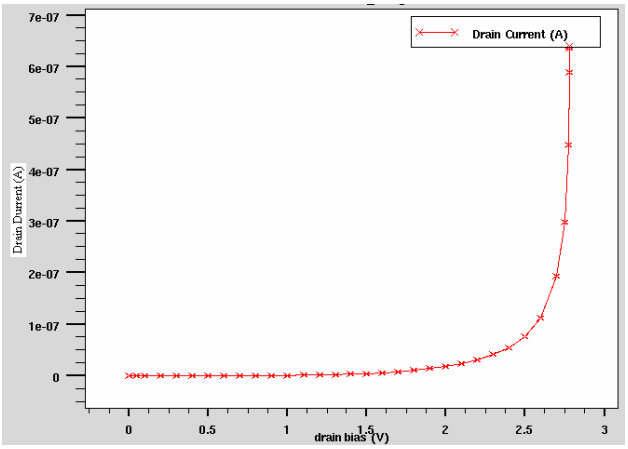


**Fig. 5**. Leakage Current of SOI MOSFET at 1 micron

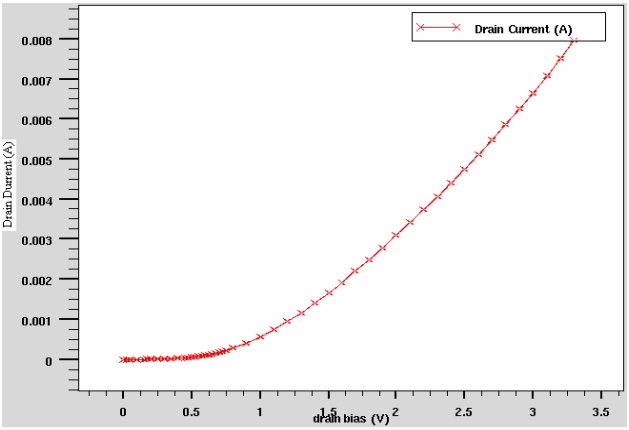


**Fig. 6.** Leakage Current of SOI MOSFET at 91nm

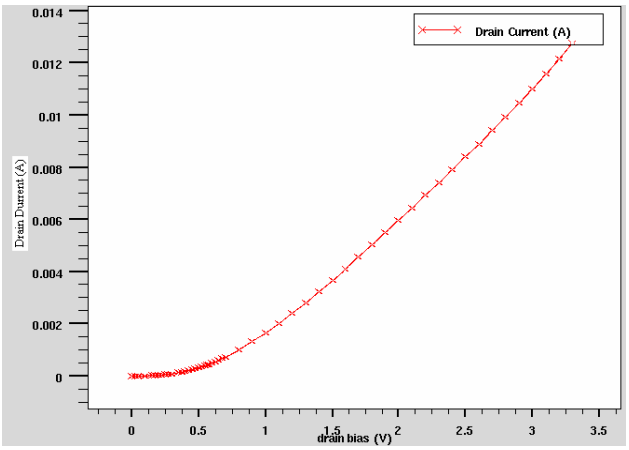


**Fig. 7.** Leakage Current of SOI MOSFET at 64nm

The plots for the extracted threshold voltage of SOI n-MOSFET at 1µm, 91nm and 64nm is as shown in fig. 8, fig. 9 and fig 10. The threshold voltage of corresponding default CMOS model from Silvaco-Athena is found to be much more than SOI models. When SOI models are

compared for different device sizes then threshold decreases as the device size shrinks as indicated by table 1.

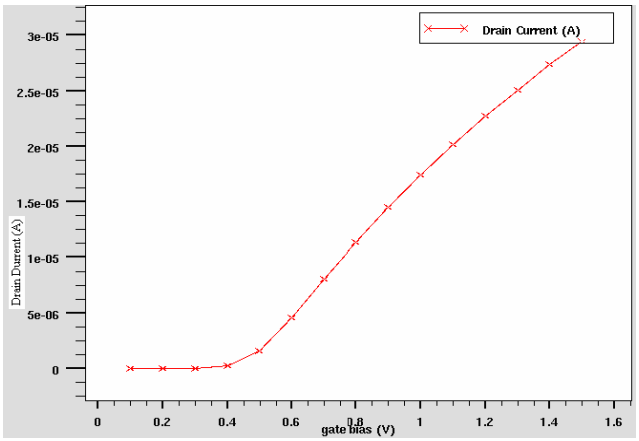


**Fig. 8.** Threshold Voltage of SOI MOSFET at 1 micron

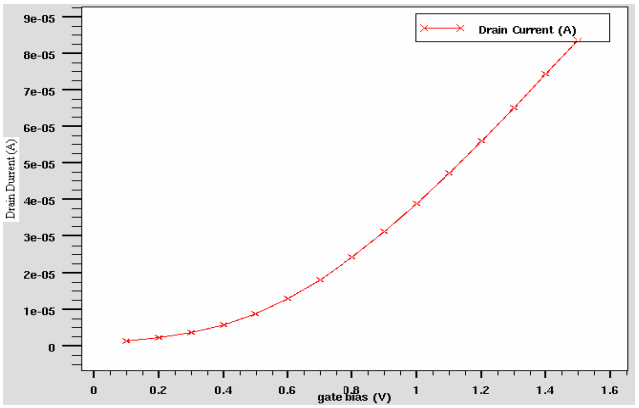


**Fig. 9.** Threshold Voltage of SOI MOSFET at 91nm

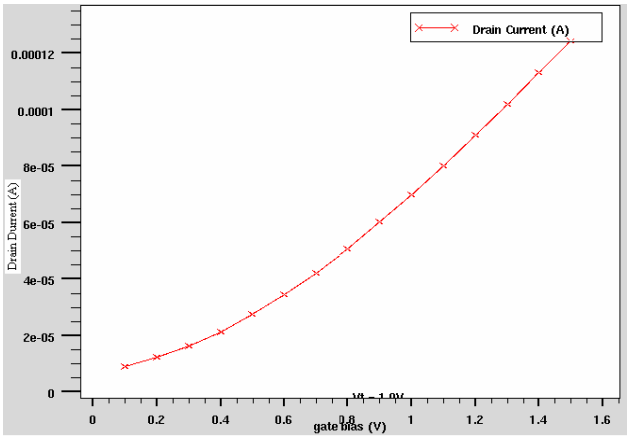


**Fig. 10**. Threshold Voltage of SOI MOSFET at 64nm

The plots for the subthreshold conduction of SOI n-MOSFET at 1µm, 91nm and 64nm is as shown in fig. 11, fig. 12 and fig 113. The subthreshold current of corresponding default CMOS model from Silvaco Athena is found to be much more than SOI models. When SOI models are compared for different device sizes then subthreshold current increases as the device size shrinks as indicated by table 1.

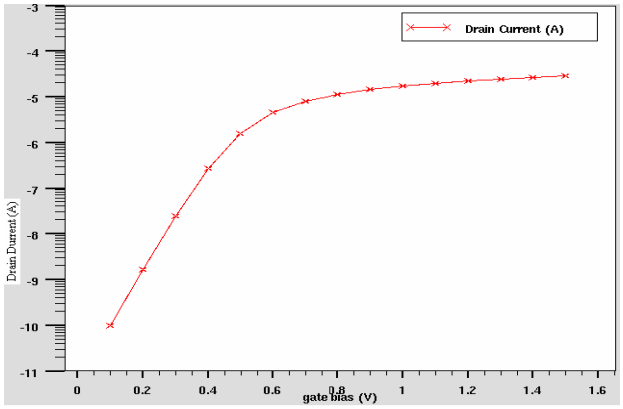


**Fig. 11**. Subthreshold Conduction of SOI MOSFET at 1 micron

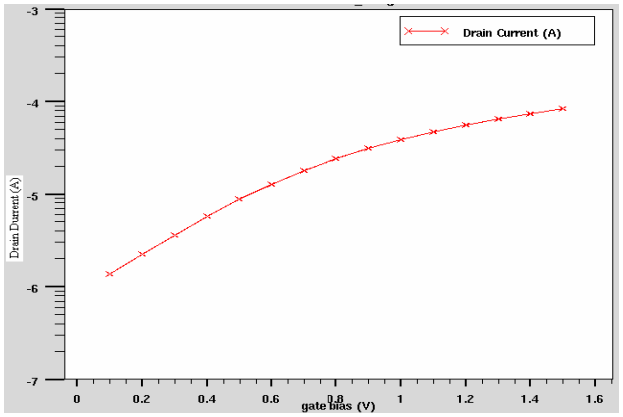


**Fig. 12.** Subthreshold Conduction of SOI MOSFET at 90nm

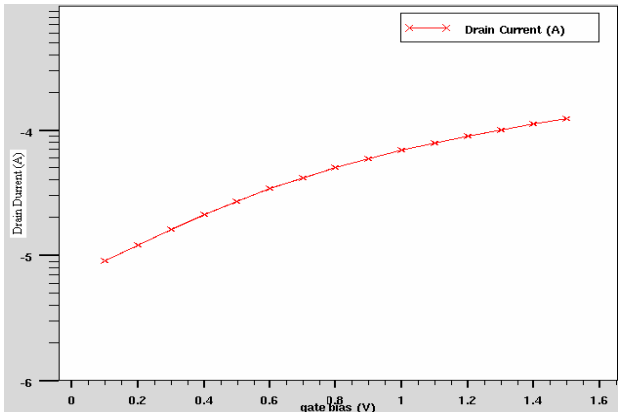


**Fig. 13.** Subthreshold Conduction of SOI MOSFET at 64nm

**Table 1** Extracted values of the leakge current, threshold voltage and subthreshold voltage at different technological nodes.

| Electrical Properties | At 0.9 micron | At 1.0 micron |
|---|---|---|
| Vth (V) | 1.01796 V | 0.496395 V |
| Sub Vth (V/decade) | 0.10675 V/decade | 0.0725169 V/decade |
| Ids_leakage(A/µm) | 1.3134e-05 A/µm | 6.04074e-14 A/µm |

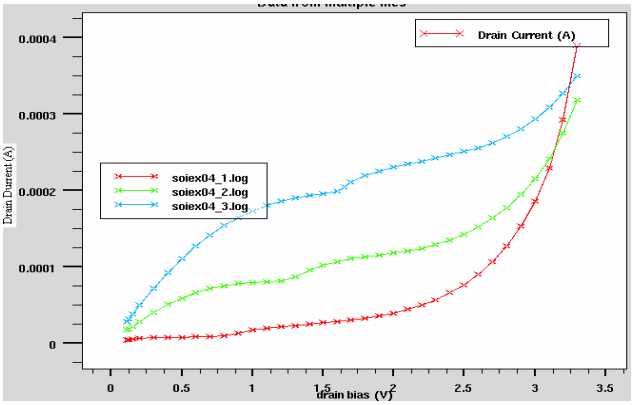


**Fig. 14.** Kink Effect of SOI MOSFET at 3micon

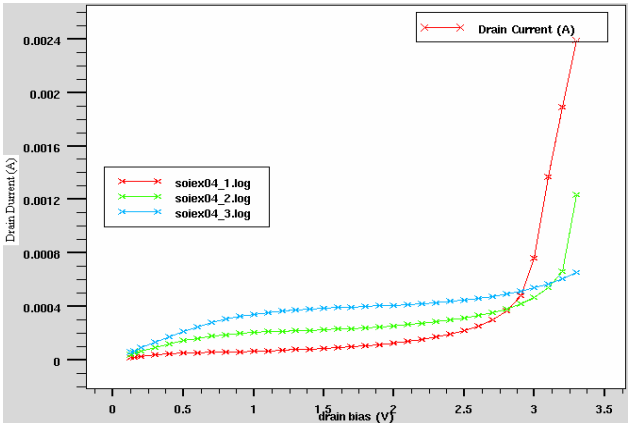


**Fig. 15.** Kink Effect of SOI MOSFET at 1micron

## Conclusion

The developed SOI n-MOSFET structure using process simulator Silvaco-Athena is compared for the various electrical properties. As compared to the bulk device n-MOSFET structure, SOI shows the improved electrical characteristics. But when scaling continues in SOI, the parasitic effects will also appear increasing the leakage current and sub threshold conduction.

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