

Research Article

A Study of N-Tunnelling Field Effect Transistor (NTFET) Through TCAD to Overcome the Technology Limitation of Conventional MOSFET

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Abstract

In this paper, it is designed and analyzed the n type tunnelling Field Effect Transistor (TFET) to obtain sub-threshold swing parameter (SS) below 60 mV/dec, it is better than the limit of conventional MOSFET. SILVACO TCAD is used for rigorous study of p-i-n structure based on Silicon. It is minimised the short channel effect of SiO₂ material. It is obtained that TFET has good ability to produce high drive current at very low supply voltage (0.1V) with very low leakage current negligible.

Keywords: TFET, band-to-band tunnelling, short channel effect, sub-threshold swing.

1. Introduction

A Tunnelling Field Effect Transistor (TFET) has capability to replace a MOSFET showing better properties over conventional MOSFET. In conventional MOSFET limitation of sub-threshold swing (SS) is limited to 60 mV/dec, while for TFET is below 60 mV/dec at room temperature. On the other hand, the TFET technology has drawback of smaller on current (I_{ON}) as compared to the MOSFET at the same channel length (L_{CH}). It has been proven that the SS parameter of the TFET depends on the gate voltage (V_{GS}), while in case of the MOSFET, it is not function of gate voltage and the physical reason is the large tunnelling barrier. TFET operated in the tunnelling dominant region where band-to-band tunneling is responsible for drain current. The tunneling mechanism occurs in drift dominant region in case of larger channel resistance (R_{CH}), in turn the drain current produces due to drift mechanism. The tunnelling especially band-to-band tunnelling (BTBT) for the p-i-n structures have been studied. Compared to the n-i-n MOSFET geometry, the p-i-n tunnel FETs (TFETs) can produce a sharper sub-threshold slope below the MOSFET limit of 60mV/decade at room temperature. This can demonstrate the lower off-current (I_{OFF}) and results lower leakage power (L_{leakage}). The on-current associated with TFET is limitation due to the tunneling barrier, which limits the p-i-n based TFET performance. As compared to n-i-n structure based MOSFETs, p-i-n structure based TFETs have performance advantages in logic circuits. It is free from short channel effects as the channel current is controlled by the tunnelling mechanism, while in conventional MOSFET technology suffers from the high short channel effect at lower dimensions.

2. Device Structure and Material Parameters

The structure under consideration is shown in Fig. 1. The device consists SOI type wafer, in which intrinsic type Silicon layer has been deposited. It is supposed that during process of creation of TFET structure, the Silicon layer has been doped p⁺-type in less than half and some portion has been protected by mask to create underneath region intrinsic. The remaining silicon region has been doped n⁺-type to create p-i-n structure laterally. After doping we have deposit Silicon Oxide material (SiO₂) to minimise the short channel effect. Over oxide material we have deposited poly-silicon for creation of Gate. It is deposited Aluminium over the P⁺- silicon, N⁺-silicon and over gate for taking the contacts for the biasing purposes named as drain, source and gate contacts.

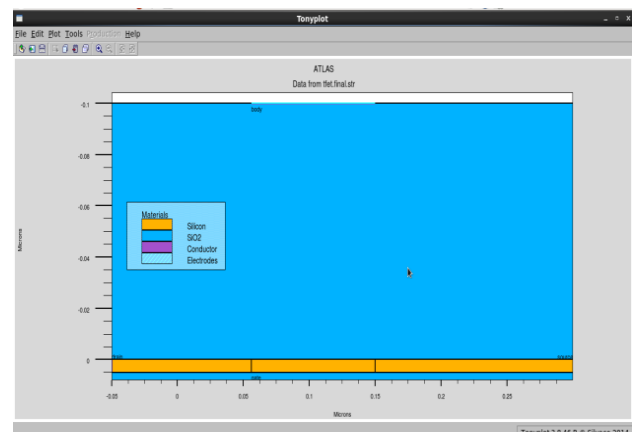


Fig.1: NTFET structure

The SiO₂ region thickness has been taken 500nm while the laterally deposited silicon thickness has been also taken

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500nm. The doping of n-type silicon has been done by the generic donors with dose $10^{18} /\text{cm}^3$, while the middle region has been doped n-type with generic donors with dose $10^{17} /\text{cm}^3$ and the p^+ silicon region has been doped with acceptor dose $10^{20} /\text{cm}^3$ as shown in Fig. 2. The standard material parameters have been taken from the SILVACO material database for silicon and oxide materials.

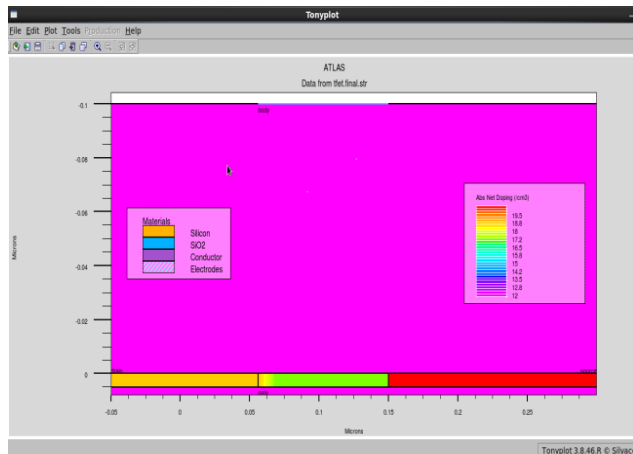


Fig.2: NTFET doping profile

A. Numerical Model

A two-dimensional numerical simulation of a homojunction p-i-n structure based field effect transistor has been done for node generate semiconductor and parabolic shape of conduction band for accurate approximation, which is in good agreement with the numerical solution in the reduced Fermi level range. It has been proved that the omission of carrier degeneracy and conduction band parabolicity will lead to enormous error in the calculation of the drain current NTFET device based on silicon material. The results presented in this work are obtained with ATLAS simulator. The Newton iteration method has been used to solve five nonlinear decoupled equations. The Newton based method improves the efficiency of the iteration.

A program has been developed for simulation of two-dimensional p-i-n FET device based on silicon. The standard formulae used in calculations of band gap energy, effective mass, mobility of charge carriers, electron affinity, SRH, Band to Band tunnelling model.

The doping of the regions has been taken analytically uniform for all three regions in the above simulation. Band-to-band standard nonlocal tunnelling model has been considered for tunnelling mechanism. The surface recombination process at the contacts has been given due to consideration in our simulation of homostructure. The quality of the interface has been characterized in terms of surface recombination velocity.

It has been taken into account the Fermi–Dirac statistics for parabolic shape of conduction band in all the calculations of carrier and doping densities. The standard bandgap narrowing effect has been considered in the analysis.

3. Results & discussions

The schematic energy band diagram of the proposed p-i-n structure based on silicon is shown in Fig. 3. The energy band diagram of heterojunction has been obtained by applying the classical theory of Anderson. From the schematic energy band diagram, it is clear electrons can tunnel from p^+ region to n^+ region as the valance band carriers of p^+ region have high energy as compared to conduction band of n^+ region. The narrow intrinsic region has been chosen to perform tunnelling mechanism. The tunnelling rate of carriers have been depicted in the Fig. 4a showing the tunnelling mechanism is dominant from p^+ region to intrinsic n-type region and Fig.4b, the graphical tunnelling rate has been shown that tunnelling is dictated under p^+ - to n- region.

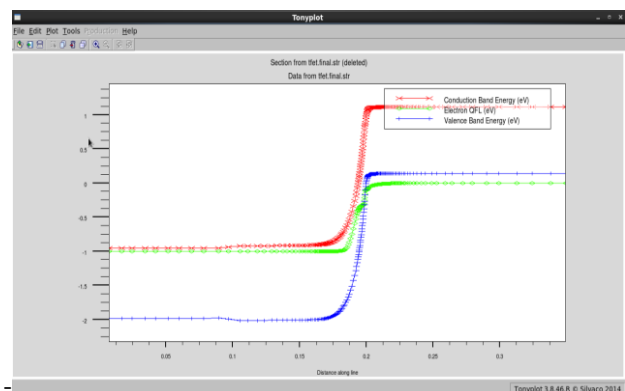


Fig.3: Schematic Band diagram with Fermi level

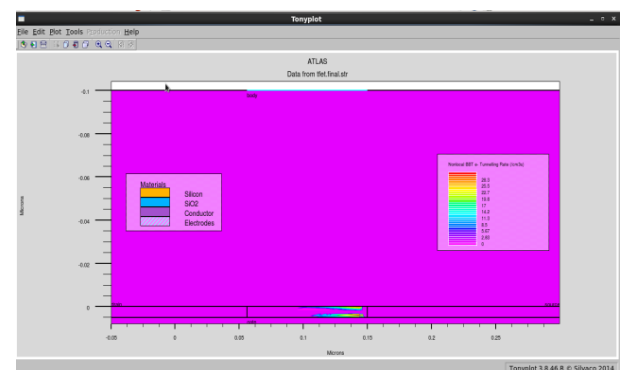


Fig. 4a: Contour of tunnelling under the structure

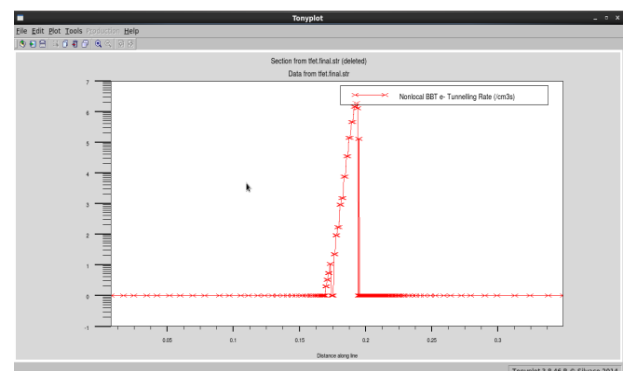


Fig. 4b: Tunnelling Rate

The electrical potential in the device structure has been depicted in the Fig. 5 under biasing condition. The maximum variation in the potential under biasing of drain and gate can be seen at p⁺-n interface, where tunnelling mechanism is dominant. The potential variation is responsible for high tunnelling of carriers from p⁺ region to n⁺ region through intrinsic n-type region.

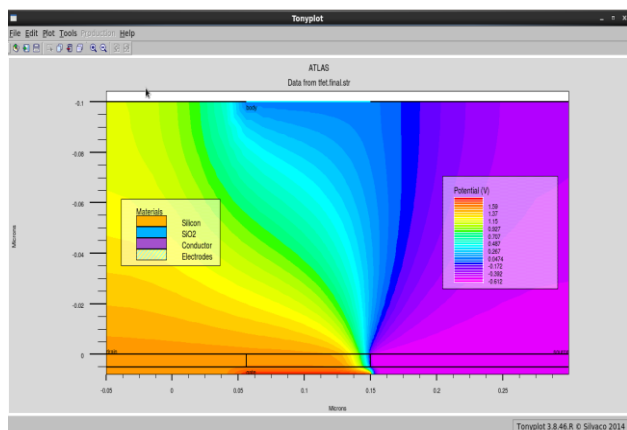


Fig. 5: Contour of Electrical Potential under the structure

Fig. 6 shows the variation in temperature with respect to carrier's product ($n \cdot p$). Due to tunnelling mechanism it is clear from the graph that temperature variation is maximum in the intrinsic n-type region as the carrier tunnelling through this region and hence increasing the temperature of the region.

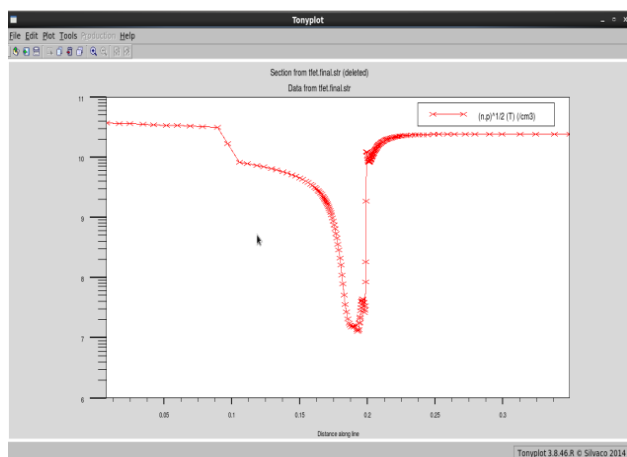


Fig. 6: Effect of tunnelling in terms of carriers product and temperature variation due to tunnelling mechanism

Fig.7 is shown here as the variation of drain current with respect to gate voltage. The tunnelling mechanism has been defined in the region assuming a square slab of dimension 0.1 micron to 0.17 micron in x-axis and 0 to .0049 micron in the y-axis shown above in Fig.1. The simulation used a dynamic nonlocal BTBT model as well as a recombination-generation is also considered for drain current calculation. The tunnelling mechanism has been controlled through the application of -0.35V to 1.15 V. However drain voltage has been fixed at 1V. The drain current shown below in fig. 7 that the NTFET reaches in

on state at almost near 0.2 V of gate current. As we increase the gate voltage beyond the 0.1 V, drain current increase in almost linear fashion. The I_d - V_G curve shows that the NTFET, which is dictated by tunnelling mechanism can be switch into ON state at very low voltage compared to conventional MOSFET which has limitations. Also, as the drain current is produce due to tunnelling mechanism, the short channel effect is negligible.

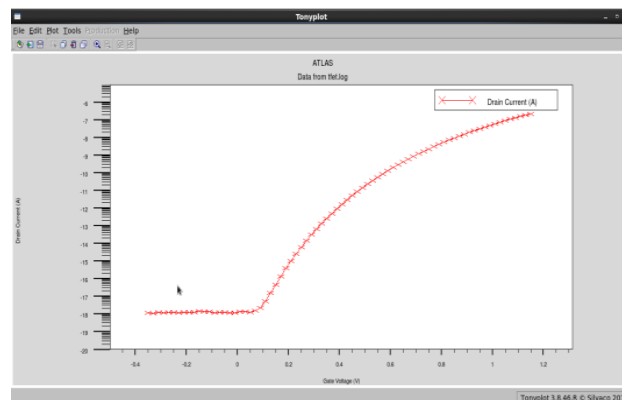


Fig. 7: Variation of drain current with respect to gate voltage

Conclusion

The present study of NTFET shows that at lower voltage we get the lower sub-threshold swing and thereby lower supply voltage needed, in turn reduce the power dissipation. This analysis requires experimental verification to understand the simulated I_d - V_G behaviour and evaluation of the potential of TFET device to replace the existing conventional MOSFET with cost effectiveness.

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