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Research Article

Implementation of CPLD Based Receiver of Telemetry device for Maternal-Fetal Monitoring

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Abstract

The advancements in the technology are driven by the customer needs and customer satisfaction, where healthcare institutions must continuously adapt in order to provide optimal patient care. One significant advancement is the development of Wireless Medical Telemetry systems for Maternal-Fetal Monitoring. With wireless systems, patients can move freely around the hospital while their physiological parameters like Uterine and Fetal activity, Fetal Heart Rate and FECG/MECG are measured. This new model of patient care is a revolutionary advancement in modern healthcare. The Telemetry system consists of a Transmitter and a Receiver unit. The transmitter can capture Uterine Activity (UA) using TOCO transducer or Intrauterine Pressure Catheter (IUPC). Fetal Heart Rate by means of Ultrasound transducers and FECG/MECG parameters are measured by the 3-lead electrode system. The captured data is then transmitted wirelessly to a receiver unit using frequency ranges within WMTS band. The key component of the receiver is CPLD which is from Altera's MAX II family. QuartusII programming tool is used to program the CPLD. The RTL schematic for enable signals for all the parameters is simulated using ModelSim. After the implementation of CPLD in the receiver main board, results are checked by measuring the values in the Fetal monitor which displays the maternal/fetal parameters.

Keywords: *CPLD- Complex Programmable Logic Device, WMTS-Wireless Medical Telemetry System, FHR-Fetal Heart rate, IUPC–Inter Uterine Pressure Catheter*

1. Introduction

Telemetry Receiver is a part of the Telemetry System that provides a wireless means of transmitting Ultrasound audio, Maternal/Fetal ECG and Uterine activity signals from an ambulatory mother to a bed side Maternal/Fetal monitor. The telemetry has special feature known as Remote Event Marker (REM) which helps in recording perceived fetal movement occurrence by the mother. The same can be observed on the strip chart and can be later analyzed by the clinician. The receiver uses an UHF RF module synthesized receiver configured at various frequency ranges. The WMTS frequency band Wireless Medical Telemetry Service (WMTS) is a wireless service specifically for transmission of data related to a patient's health.

Discrete logic devices have been used regularly in the semiconductor industry had a unit cost advantage over programmable logic devices for several years. However, times have changed significantly. Advancement's in semiconductor processing technology for CPLD's have driven the costs of these devices down to a point where they now are a discrete logic replacement alternative. The key component in the receiver is CPLD which is from Altera's MAX II family. QuartusII programming tool is used to program the CPLD. The RTL schematic which are simulated using ModelSim software are used to validate the design. After the implementation of CPLD in the receiver the results are checked by measuring the values in the Fetal Monitor which displays the Maternal/Fetal parameters.

A. Maternal-Fetal ECG

One of the non-invasive assessment of fetal well-being is using fetal electrocardiogram (FECG) recorded on the maternal abdomen for fetal monitoring during pregnancy. However, the FECG signal recorded on the abdominal wall is weak and nearly always overwhelmed by the various kinds of interference such as the maternal ECG (MECG), power line disturbance, and baseline drift due to respiration. Among these interferences, the MECG dominates all the other signals. The FHR can be obtained by detecting the Fetal R waves after the MECG is removed from the abdominal ECG. Nevertheless, it is very difficult to completely separate out the MECG thanks to the overlapping of FECG and MECG in both time and frequency domain (A. Fanelli *et al*, 2011).

There is a standard placement of electrodes while performing ECG recordings called a standard bipolar limb lead. A lead refers to the potential difference between two electrodes. Lead placement involves three leads, which are

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placed on the right arm (RA), left arm (LA) and left leg (LL). The electrodes can be attached to the wrists and inner ankle, but for clinical applications, are usually attached to the chest for a more accurate signal. Lead I, II and III constitute the standard limb lead ECG. Using these three leads, we can form what is called Einthoven's triangle

Adaptive filtration and matching filtration are one of the classical methods. Although these two methods takes into account the spatial features of the abdominal ECG and could provide more robust separation of abdominal MECG, multiple channels of ECG data have to be acquired from the abdominal wall. The maximum amplitude of the QRS usually oscillates from 100µV to 150µV for the maternal recording and up to 60µV for the Fetal recording.

B. Fetal/Maternal Heart Rate

The present day medicine is characterized by the development of new measurement methods which should be more efficient, less invasive and in case of long lasting monitoring less annoying for a patient. Operation principle of these methods is based on measurement of duration of Fetal cardiac cycles. In Fetal electrocardiography (FECG), this duration is represented by TRR interval between two consecutive R-waves. The Fig 1 shows the Matlab implementation of ECG signal sampled at 100 Hz and the peaks (P, Q, R, S, T and U) marked. The signal of good quality allows detection of R-waves using quite simple algorithm based on peak detection. In Doppler US technique, heartbeats are detected from the envelope of US wave reflected from moving parts of Fetal heart-valves or walls. Peak detection can provide incorrect data due to complex and unstable shape of the envelope signal. Therefore, for the detection of consecutive heartbeats the correlation techniques considering full shape of the analysed signal are applied. Auto correlation with adaptive window selection or cross-correlation with changeable template is mostly used (Chang Su Lee,*et al*,2009). Distance between two consecutive peaks of auto correlation function corresponds to the interval between two consecutive R-waves in electrocardiogram.

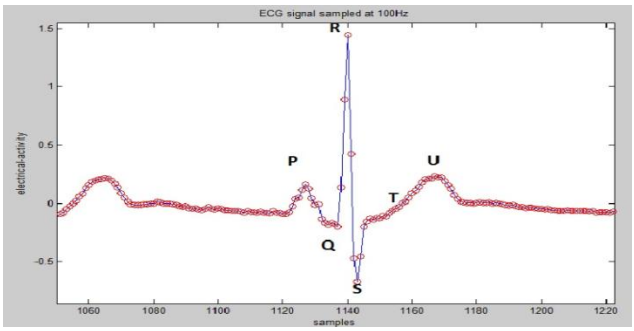

Fig 1:ECG waveform simulated using Matlab

Values of TRR intervals are transformed into instantaneous Fetal heart rate (FHR) expressed in Beats Per Min (BPM) accordingly to the equation: FHR[BPM]=60000/TRR [ms]. Such data set creates a signal of Fetal heart activity, which as printed waveform is visually analysed by a clinician (M.A.Hasan, *et al*,2011).

The Ultrasound transducers are built using 9 piezoelectric crystals of 1cm in diameter, one positioned centrally and the others in a circle around it. The working frequency is equal to 1.151 MHz and the acoustic power of the ultrasound wave does not exceed 1.5 mW/cm^2. The ultrasound transducer is placed on mother belly (Janusz Jezewski, *et al*,2006).

C. Uterine activity of Mother

Fetal distress syndrome is an abnormal condition during gestation or at the time of delivery, marked by altered heart rate or rhythm and leading to compromised blood flow or changes in blood chemistry. Cardiotocography is the common non-invasive diagnostic technique utilized in obstetrics to detect and determine the extent of Fetal distress syndrome. A low cost disposable Toco sensor consists of pressure transducer configured in a Wheatstone Bridge is used for contraction monitoring and an instrumentation amplifier with a gain of 100 amplifies the signal to the ADC input range. There are two ways of measuring and they are 1. External method and 2 . Internal method

In external method the pressure sensitive contraction i.e. a Tocodynamometer (Toco) has a flat area that is fixated to the skin by a band around the belly. The pressure required to flatten that section of the wall correlates with the internal pressure, thereby providing an estimate of it.

The internal method involves inserting a pressure catheter, the uterine catheter into the uterine cavity, internal measurement is more precise, and might be preferable when a complicated childbirth is expected. The Toco device identifies the frequency of contractions, but not their intensity and suffers both from misalignment following maternal movement and technical limitations in obese patients.

D. WMTS-Wireless Medical Telemetry System

The Wireless Medical Telemetry Services (WMTS) band was established by the FCC in the United States for transmission of data related to a patient's health and similar reserved channels exist for life-critical communications throughout the world. The WMTS constitute 608-614 MHz, 1395-1400 MHz and 1427-1432 MHz. Some wireless telemetry system can also operate in the ISM (Industrial, Scientific and Medical) band. WMTS uses traditional narrow band transmission and spread spectrum. The narrow band transmission allows for a 25 or 50 kHz spacing channel separation. It provides 240 different channels for 25 kHz channel spacing and 120 channels for 50 kHz spacing. This is possible because of the 6 MHz band space available in the WMTS band. This type of transmission, in the WMTS band is a good option for smaller-sized hospitals.(Rahman Doost-Mohammady *et al*,2012; Kaushik.R.Chowdhury *et al*,2012)

The spread spectrum transmission is used in the WMTS and ISM telemetry systems. Some WMTS systems

used what is called the "frequency hopping spread spectrum". Some medical telemetry system manufacturers are capable of providing a smaller channel separation, which increases the availability of different channels. (MasoudRoham, *et al*,2011; Mehmet R Yuce, *et al*,2008*).*

E. CPLD, Enable Signal Generation, In-Circuit Programming

7400-series devices had low costs relative to CPLDs. However, once again, technology improvements have rewritten the cost equation, allowing CPLDs to gain equal, if not better, costing against TTL devices. That is, the unit costs of CPLDs have been driven down to the point where they are below to those of discrete logic devices. Factoring in the high hidden costs underlying discrete logic devices-which include increased inventory, high power consumption and EMI, low reliability, prolonged time to market, and higher maintenance makes CPLDs the clear, superior alternative to discrete 7400 series devices.

2. Main Board of the Telemetry Receiver

A. Major Blocks in Telemetry Receiver

There are 8 supply lines are provided to the main board from the power supply board i.e. SMPS Board. An eight pin header is provided for the same on the main board. The supply lines are +15V, -15V, +12V, +5V, -5V, +3.3V, +1.8V and Ground reference. There is an antenna which is equipped on the receiver panel to capture the data sent from the transmitter. Through a cable and SMB connector, the signal is fed to the receiver module mounted on the main board. The main board of the Telemetry Receiver and the functional blocks are shown in the Fig 2.

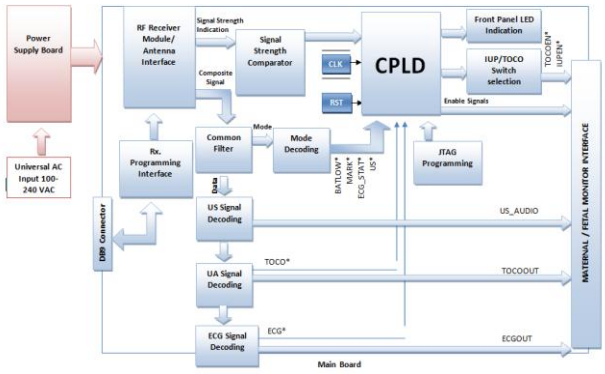

Fig 2: Main Board of Telemetry Receiver

The receiver module is configured at a frequency rangebetween 608-614 MHz with a Center frequency of 611 MHz. The Transmitter and Receiver have to be programmed to the same frequency range.

B. Signal Strength Comparator

This section is realized using voltage divider circuit which is an Ultra-Low Power Quad Comparator from National Semiconductor.

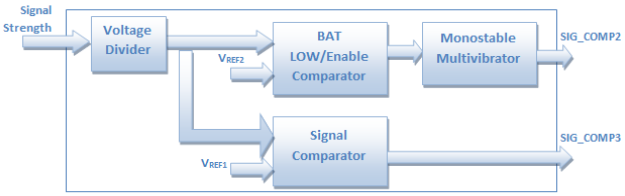

Fig 3: Signal Strength and Multivibrator block

Signal Comparator is provided to define the stable signal strength area. Here the inputs are same as the ones given to BAT LOW/Enable comparator except that the reference level is slightly higher than the one set for BAT LOW/Enable comparator. The reference signal bypasses the divider logic. The blocks have been indicated in the Fig 3.

Let us consider the reference signal for Signal Comparator as $\mathbf{V_{REF1}}$.Here, $V_{REF1} = V_{REF}$ as against the $V_{REF2} = V_{REF}$ *2/3 level considered for BAT LOW/Enable comparator. This leads to a different threshold level for Signal Comparator. When V_{IN} is greater than V_{REF1} the output of Signal Comparator will be LOW and when V_{IN} is less than V_{REF1} the output will be HIGH. The point to be noted here is that the output of Signal Comparator becomes LOW at a later time than BAT LOW/Enable comparator but during the reverse process, it becomes HIGH well before BAT LOW/Enable comparator output becomes HIGH.

The output of Signal Comparator is referenced as SIG_COMP3**,** which is pulled up to 3.3V through 4.99KΩ. Simultaneously; a square wave is generated within the CPLD, referred as 1.3 sec Pulse. This signal is NAND'ed with Signal Comparator output to generate the LED indication. The output variation in BAT LOW/Enable comparator and signal Comparator indicates that the signals strength is weak in this region and hence the LED flashes. The continuous LOW level in both these outputs indicates high signal strength and the LED will be ON. When continuous HIGH level is detected in these outputs LED will be OFF, indicating no communication between receiver and transmitter.

C. ECG Signal Decoding

The composite signal from the module consists of various frequency components and they have to be filtered out separately to divide them into ECG, UA and US. Filtered ECG signal, estimated in 2.45KHz to 2.95KHz frequency range, is passed through an ECG decoder circuit which reproduces the exact ECG signal transmitted from the transmitter unit. This is basically an FM detector/Tone detection circuit. FM detector reproduces the signal whereas the tone detection part generates an active low signal when ECG signal information is present in transmitted signal. ECG enable signal for Maternal-Fetal monitor is derived from this tone signal.

D. UA and US Signal Decoding

Uterine activity (UA) is the signal obtained using an IUP

transducer or a TOCO transducer attached to the patient. The selection of respective enable signals, to Maternal/Fetal monitor, depends on the position of IUP/TOCO switch, which is a manually operated rocker switch on the front panel.UA frequency range is expected to be from 1.5KHz to 2KHz. Its decoding from composite signal involves aseries of filters, Tone decoder, amplification followed by a gain and offset adjustment.

Ultrasound signal is a part of the composite signal which is expected to be in 200Hz to 500Hz frequency range. US decoding comprises of a series of filtering sections, frequency halver circuit and a final amplification part.

3. Test Setup and CPLD Characteristics

The test setup consists of a Fetal Simulator which will provide real time signals like ECG, UA and US to the Transmitter. The signal is wirelessly transmitted to the receiver where the signals are captured and it is displayed on the Fetal monitor. The Fig 4 indicates the Telemetry test setup. The instruments used in the setup are

1. Telemetry Transmitter
2. Fetal Simulator

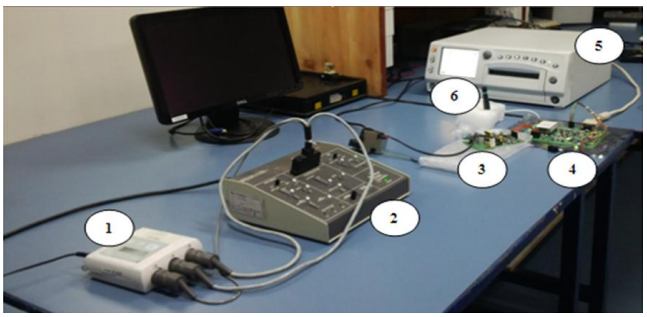

Fig 4: Telemetry Test Setup

3. Telemetry Receiver Main Board
4. SMPS Board
5. Fetal Monitor
6. Portable Antenna

CPLD family used in the receiver is Altera's MAX II family. MAX II devices have lower price, lower power and higher density which make them the ideal solution for complex control applications, including new applications not previously possible in CPLD. The high density of MAX II CPLD's gives designers the added logic necessary for controlling complex, system-critical power-up sequences. Power-up sequencing is the process of supplying power to other devices on the board in a sequence, ensuring that all devices operate correctly. A JTAG port can also be used to monitor the power-up sequence and identify any errors via the JTAG port to the PC or test equipment. The JTAG port can also be used to set break points in the power up sequencing, reducing engineering time during the board level debug and verification process (ZhiDeru, *et al*, 2010).

MAX II devices are supported by Altera's Quartus II software, the easiest-to-use software for CPLD design. The Quartus II software provides a number of tools to enable the simple and easy design of MAX II devices. The CPLD has 240 logical elements. VHDL behavioural programs are written in Quartus II software based on the requirement. The RTL schematics are validated using software known as ModelSim which is part of Altera's Simulation tool. Once the results are validated and tested, the (.pof) file is generated and the program is burnt onto the receiver which has CPLD in it via USB Blaster shown in figure 5a and 5b. The test setup is then made ready and tested on fetal monitor to display the parameters and the waveform on the screen, flowchart for the same is shown in Figure 6.

(a)

(b)

Fig. 5 (a): CPLD chip **Fig. 5 (b)** USB Blaster

VHDL is commonly used to write text models that describe a logic circuit. Such a model is processed by a synthesis program, only if it is part of the logic design. A simulation program is used to test the logic design using simulation models to represent the logic circuits that interface to the design. This collection of simulation models is commonly called a testbench.

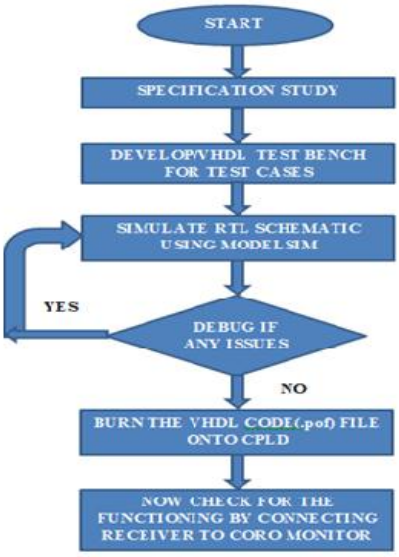

Fig. 6: Flowchart for implementation of the code

Register-transfer level (RTL) is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals (data) between hardware registers, and the logical operations performed on those signals. RTL is used in VHDL to create a high-level representation of a circuit, from which a lower-level representation and actual wiring can be derived. The input and output port are mapped in CPLD as shown in figure 7.

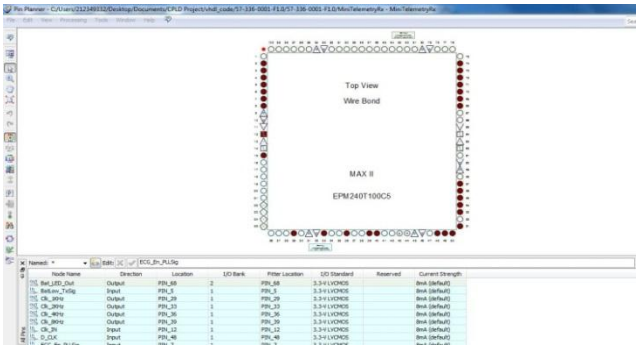

Fig 7: CPLD Pin mapping

4. Simulation Results on Altera's ModelSim

All signal inputs to the CPLD are registered at the falling edge of input clock. This is to avoid processing any glitches in the input signals. The code is divided into two, first program is written for clock generation and the second program is for enable signal generation.

A. Clock Generation

Divided clocks are generated using a 15bit binary counter. The output of the counter is taken as Count_B14, bits being 0 to 14. 32.768KHz is the input from Crystal oscillator. Hence Bit(1) forms the 8.192 KHz clock. Bit (1) gives the divided by four of the input clock. Bit(2) forms the 4.096 KHz clock, which is the divided by eight of the input clock. Bit(3) gives the divided by 16 of the input clock, i.e. 2.048KHz. Bit(4) makes the divided by 32 of the input clock which is 1.024 KHz. These are the clocks fed to the respective filter building blocks that work as 80Hz, 40Hz, 20Hz and 10Hz Bandpass fourth order filters.A 15 bit counter is used for generating divided clocks, considering the additional requirement of 0.75Hz pulse generation. Bit(10) gives the 16Hz pulse. This 16Hz is given as input to a 4 bit counter 'Count_B4' which is made to count up to 10. Bit (3) of Count_B4 gives 0.75Hz (1.3 sec) signal. The clock generated RTL schematic is shown in Fig 8.

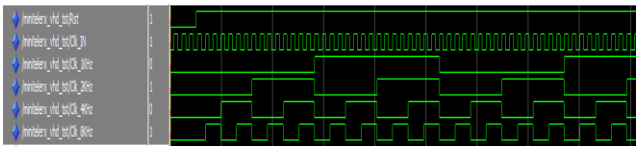

Fig 8: Clock generation RTL schematic

B. Signal strength LED Indication

This indication is such that the LED shall be continuously OFF when the signal strength is too LOW or the signal is not available. It shall be continuously ON when the signal strength is HIGH and LED shall be flashing when the signal strength is weak. The LED indication for signal strength shall be carried out by comparing the Sig_Compare_2 and Sig_Compare_3 signals from the Mono-Stable Multivibrator &Comparator respectively. The registered Sig_Compare_3 signal shall be NAND'ed with the 1.3 second generated pulse resulting in a pulsed output when Sig_Compare_3 is HIGH and the output shall be HIGH when Sig_Compare_3 is LOW. The output of this gate is again NAND'ed with the Sig_Compare_2 signal to generate the LED OFF as shown in Figure 9 and 10.

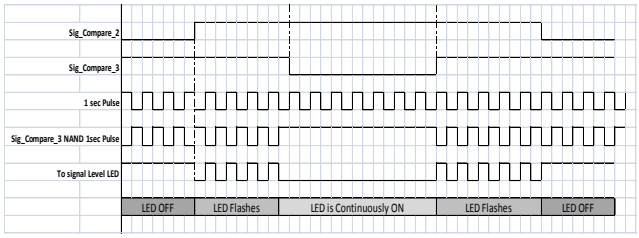

Fig 9: Signal Level LED Logic diagram

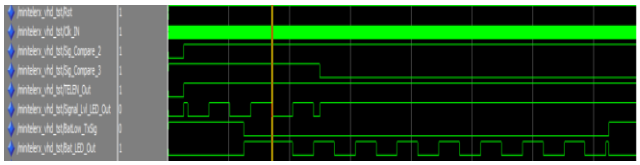

Fig 10: Signal strength and battery Low LED RTL Schematic

C. Battery low LED Indication

Battery Low LED indication is such that when the active low battery low information (BatLow_TxSig) from the transmitter is HIGH, the LED will be OFF. When the signal is LOW (meaning low battery)and none of the sensing signals like ECG, UA and US are enabled, the battery low LED will be continuously ON.Again, when the signal is LOW and the sensing signals are ON, then the LED will be flashing as shown in Fig 9 and Fig 10.

This shall be implemented by inverting the battery low signal and then NAND'ing with the 1.3 sec_Pulse to generate the flashing region of the LED. The inverted battery low signal shall be again NAND'ed with the sensing signals' enable lines so that when none of them are enabled (in HIGH state), the output of the NAND gate will be LOW. This when combined with the signal strength input (Sig_Compare_2), keeps the LED continuously ON. If the signal strength is low (Sig_Compare_2=0) then Battery low LED will be turned OFF.

D. ECG signal generation

This refers to two types of ECG enables viz. Maternal MECGEN_Out and Fetal FECGEN_Out. Generation of ECG enable signals shall incorporate the ECG_status signal from transmitter, active low ECG enable signal from Tone decoder/PLL and the signal strength information. ECG status from transmitter indicates whether the transmitted signal is a maternal ECG or fetal ECG i.e. '1' indicates MECG and '0' indicates FECG.

As long as signal strength is HIGH and ECG_EN_PLLSig (active low) is LOW, MECGEN_Out

shall be '1' if ECG_Stat_TxSig is '1' and FECGEN_Out shall be '1' if ECG_Stat_TxSig is '1'.These outputs shall be driven through NPN transistors to provide active low telemetry enable signal to Maternal/Fetal Monitor. Refer Fig 11 for the RTL Schematic.

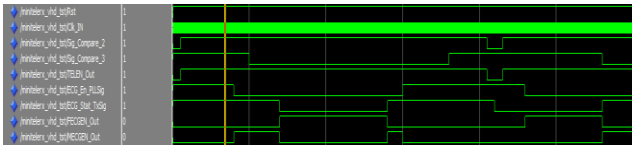

Fig 11: MECG/FECG Enable Signal Generation RTL schematic

E. US signal generation

USEN_Out shall be generated by NOR'ing the monostable multivibrator output (inverted) and the US enable signal from the transmitter. This indicates that as long as transmitted signal is stroung enough and the US enable signal from the transmitter is LOW (active low), then USEN_Out is HIGH as shown in Fig 12. This output shall be driven through an NPN transistor to provide active low telemetry enable signal to Maternal/Fetal Monitor.

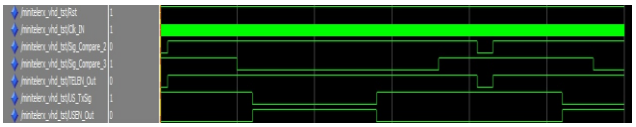

Fig 12: US Enable Signal Generation RTL Schematic

F. UA Enable Signals

As far as UA signal generation is concerned, UA_Enable signal and its inverted signal shall be provided by CPLD. UAEN_Out is generated by NOR'ing the inverted signal strength information from monostable multivibrator and the active low enable signal (UA_En_PLLSig) from PLL. When both these signals are LOW, UAEN_Out will be HIGH as shown in Fig 13. This signal shall be passed through an NPN transistor to provide active low UA enable signal to Maternal/Fetal Monitor.

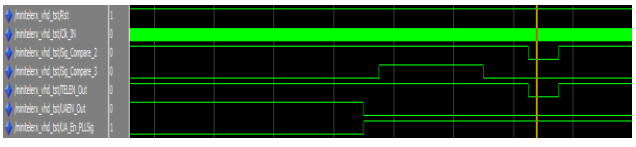

Fig 13: UA Enable Signal Generation RTL Schematic

Conclusion

Measurements on Maternal/Fetal Monitor

After the simulation results are validated, the program is loaded onto the CPLD. Finally the connections are made according to the test setup shown in Fig 4. The readings are set through the Fetal Simulator, which is then given to the transmitter and the parameters are transmitted to the receiver. The signal received by the receiver is then sent through Maternal/Fetal monitor and the parameters are displayed on the screen as shown in Fig 14. The FECG reading of 240BPM is displayed along with its waveform, Ultrasound reading which is nothing but the Fetal Heart rate of 50BPM and Uterine Activity reading of 69mmHg is displayed on the Maternal/Fetal monitor. It is to be noted that the product is intended for use by clinical professionals who are expected to know the medical procedures, practices and terminology required to monitor obstetrical patients and that the final call has to be taken by the clinician regarding the status of the patient.

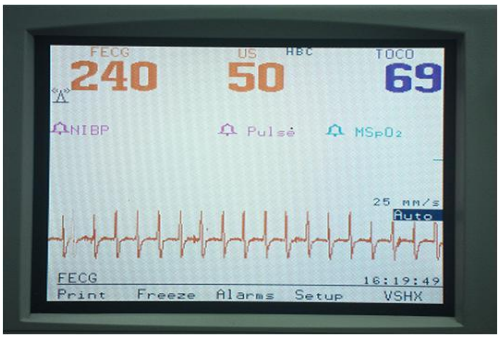

Fig 14: Maternal/Fetal Monitor Displaying Maternal/Fetal parameters

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