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Research Article

Design of VHDL based Multi-Directional Sobel Edge Detection Processor

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Abstract

Aim of the system is to develop a field programmable gate array based edge detection system. The proposed system calculates horizontal edge, vertical edge, left diagonal edge and right diagonal edge of gray scale image. Synthesizing and Simulation results and proposed Sobel edge detection system on Xilinx Spartan3 XC3S200 FPGA chip demonstrate the efficiency of proposed architecture for edge detecting of gray scale images for real-time image processing applications.

Keywords: *Vhdl, Sobel Algorithm, Edge Detection, FPGA.*

1. Introduction

Edge detection means finding the edges of the image according to the intensity variation of each pixel. This characteristic of edge detection gives much application in image processing as well as computer vision applications. There are some well-known methods for edge detection such as Prewitt, Canny, Sobel, and Roberts algorithms which are different in terms of performance on hardware, speed and simplicity. The Sobel operator is mainly used for hardware implementation due to efficiency and simple mathematical model that make it easy for real-time edge detection applications. The edge detection is mainly applicable in case of data transmission; in that case the edge detected data reduce the amount of data to be transmitted (Amala Ann Augustine et al, 2013). In this system Sobel edge detection method is used. Threshold value is fixed to compare with each of the gradient value for detecting if the pixel under consideration is an edge or not. It is also necessary set a threshold value to have an upper and lower limit. Upper threshold will be helpful to detect the edges and lower threshold will recognize the curves in the image. Here the edge detection is a gradient approach. So the first derivative of each pixel is taken and calculated the gradient value for that pixel this Value is then compared with threshold values if it is above than threshold then it is an edge if it is below than threshold then it is not an edge (G.Anusha et al, 2012). Edge is detected in accordance with the intensity variation, if high change in the value of intensity then there is an edge.

The intensity value is constant, and then derivative value is zero and there is no edge. Along with Sobel edge detection there are many methods to find edges Of an image. As Compared to other methods it has been found that edge detection by Sobel method is less complex and easy for computation.

2. Field Programmable Gate Array

Field Programmable Gate Array (FPGA) technology has become an alternative for the implementation of software algorithms. The unique structure of the FPGA has allowed the technology to be used in many applications from video surveillance to medical imaging applications. FPGA is a large-scale integrated circuit that can be re-programmed. The term "field programmable" refers to ability of changing the operation of the device and gate array having ability to makes reprogramming possible of an internal architecture of device. Implementations of real-time image processing algorithms can be done on general purpose microprocessors (Sanjay Singh et al, 2012). The application of FPGA in image processing has a vital impact on image or video processing. This is due to the potential of the FPGA to have parallel and high computational density as compared to a general purpose microprocessor.. During the recent years FPGAs have become the dominant form of programmable logic.

3. Sobel Edge Detection Method

In Sobel Edge Detection there are two masks, one mask identifies the horizontal edges and the other mask identifies the vertical edges (Samta Gupta, Susmita Ghosh et al, 2013).

The mask which finds the horizontal edges that is equivalent to having the gradient in vertical direction and the mask which computes the vertical edges is equivalent to taking in the gradient in horizontal direction. Sobel 5*5 masks are given in the figure 2.By passing these two masks over the intensity image the gradient along x

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direction (Gx) and gradient along the y direction (Gy) can be computed at the different location in the image.

P1	P2	P3	P4	P5
P6	P7	P8	P9	P10
P11	P12	P13	P14	P15
P16	P17	P18	P19	P20
P21	P22	P23	P24	P25

Fig.1 A typical 5×5 Image mask

EH =

5	8	10	8	5
4	10	20	10	4
0	0	0	0	0
-4	-10	-20	-10	-4
-5	-8	-10	-8	-5

EV =

-5	-4	0	4	5
-8	-10	0	10	8
-10	-20	0	20	10
-8	-10	0	10	8
-5	-4	0	4	5

Fig. 2 Sobel Operators

Now the direction of the edge at that particular location can be computed by using the gradients Gx and Gy. The gradient of an image is defined as the vectors (Varun Sanduja et al, 2013)

$$\nabla f = \begin{bmatrix} G_x \\ G_y \end{bmatrix} = \begin{bmatrix} \frac{\partial f}{\partial x} \\ \frac{\partial f}{\partial y} \end{bmatrix}$$

Where Gx is the partial derivative of f along x direction and Gy is the partial derivative of f along the y direction. Finding the magnitude of the gradient involves squaring the two components Gx and Gy adding them and taking the square root of this addition shown below

$$\nabla f = mag(\nabla f) = [G_x^2 + G_y^2]^{1/2}$$

The magnitude of the gradient to be sum of magnitude of Gx gradient in the x direction plus magnitude of Gy in the y direction which are shown below

$$|G| = |G_X| + |G_Y|$$

This method calculate gradient just in vertical and horizontal direction but for more accuracy we can do this in diagonal directions. The gradient of the image in all pixels and in all directions should be calculated for detecting the edges i.e. (EH, EV, EDL, EDR) (Arash Nosrat et al, 2012). There are two ways in these cases; spotting hypothetical required neighbors (black or white) for that pixel and calculate the gradient for the pixel or spotting constant value gradient for these pixels that mean there is no edge in these pixels.

4. Design Methodology

This paper purposed Edge Detection using Sobel Operator in Digital Image Processing and implementation using VHDL. The Design Methodology of Sobel Edge Detection algorithm shown below it consists of various steps to find

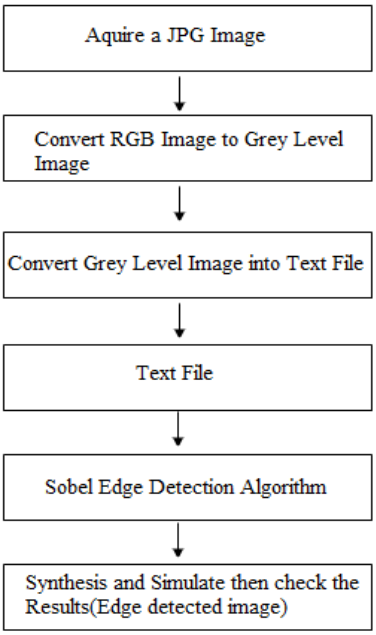

Fig.3 Process Flow of Edge Detection

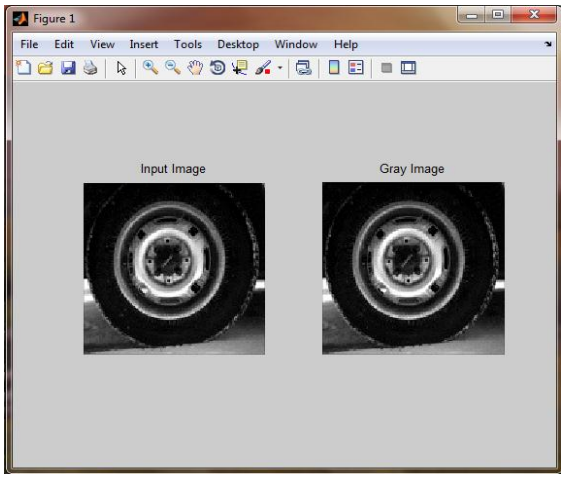

Fig.4 Input and Grey Image

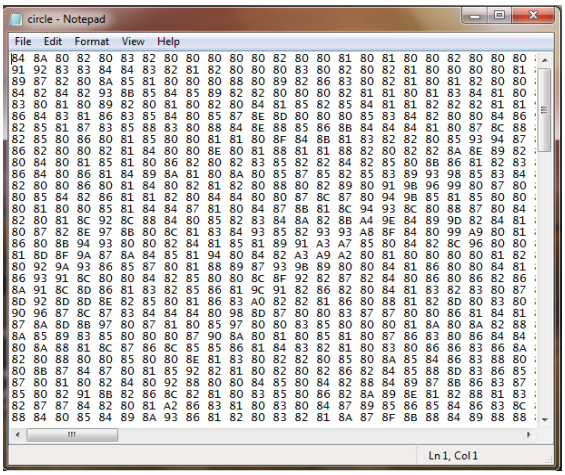

Fig.5 Text File of Input Image

the Edges of the image. Firstly, a jpg image is inputted and converted into grey image with the help of MATLAB a jpg image, which is by default in an RGB color space and convert this RGB image to grey level image .This grey image is very large, so it is resized and written into a text file as shown in the figure5.

Further implementation is done on the Xilinx ISE 13.1 and Modelsim.This Text file is an input to the Sobel Edge Detection algorithm which consist of several blocks as shown in figure6.

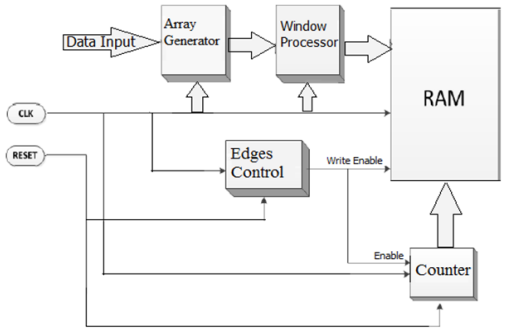

Fig.6 Hardware Architecture of Sobel Algorithm

4.1 Array Generator

The input image data comes from a text file in serial format using a synchronous clock. The input data is entered into array generator block and this block arrange data in 5*5 array format. Then gradient calculations on input data should be done. Five cascade shift register performs the gradient calculations. For example, assume that the size of input arrays is M×N where M and N are the total numbers of rows and columns of digital image respectively. The size of first shift register should be five pixels and size of second, third, fourth and fifth ones should be N pixels respectively and at every rising edge of clock, one input pixel enters into shift registers of array generator (Rajesh Mehra & Rupinder Verma et al, 2012). Therefore after 4N+5 clocks the specified pixels (P1 to P25) can be used as the input pixels frame where P13 is the center pixel.

4.2 Window Processor

The produced pixels frame (P1 to P25) by the 5×5 Array Generator block is the input of Window Processor block which calculates the gradient values based on Sobel operator for pixel P13 in all directions for detecting edges. Therefore Four parameters (EV, EH, EDL&EDR) will be produced for each frame pixels. This block contains four segments that each of them calculates the Edge in one direction and then the Edges in four directions are produced concurrently and Edge of the images are stored in RAM Block.

4.3 Edges Control

The structure of edges control module is shown in Fig. 4. Clk is the clock signal and Reset is the reset signal. Turn is enable signal when the Turn is valid the module works. EN is the output data control signal and this block can know where the current pixel location is and whether it is the edges of the image (Sanjay Singh et al, 2012). Furthermore, it controls the counter that generates the addresses for the RAM block.

4.4 Counter

Counter block count the number of rows and columns of input image i.e. input text file and produced appropriate addresses for the RAM block to save the resultant output images pixels data from the window processor. As the width of pixels is eight bits, so for every address six 8-bit data are saved.

5. Simulation Results

This section provides some simulation results for implementing the proposed Sobel edge detection processor on Xilinx Spartan3 XC3S200 FPGA chip. The ISE13.1 is used for synthesizing the VHDL modeling codes and the device utilization summary is shown in fig 7.

Resource	Used	Available	Device usage
Number of Slice Flip Flops	128	3,840	3%
Number of 4 input LUTs	207	3,840	5%
Number of occupied Slices	154	1,920	8%
Number of Slices containing only related logic	154	154	100%
Number of Slices containing only related logic	0	154	0%
Total Number of 4 input LUTs	297	3,840	7%
Number of bonded IOBs	28	141	19%
Number of BUFGMUXs	1	8	12%

Fig.7 Device utilization summary

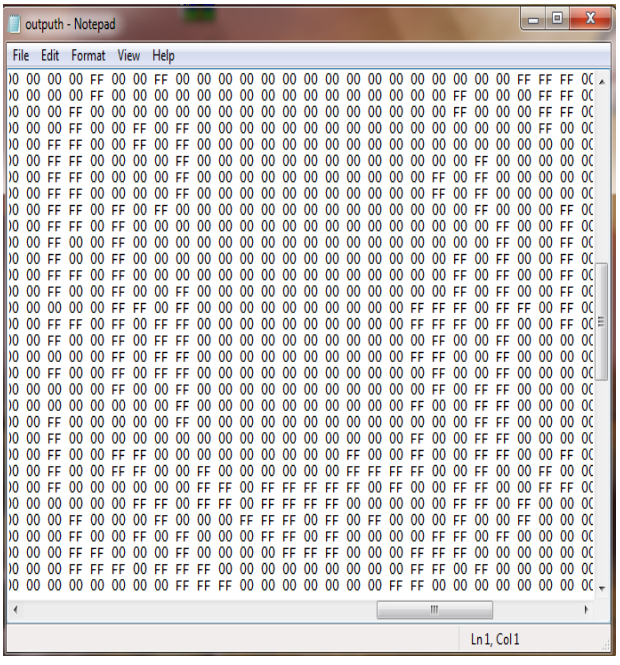

Fig.8 Output Text File of Horizontal Edge detected image.

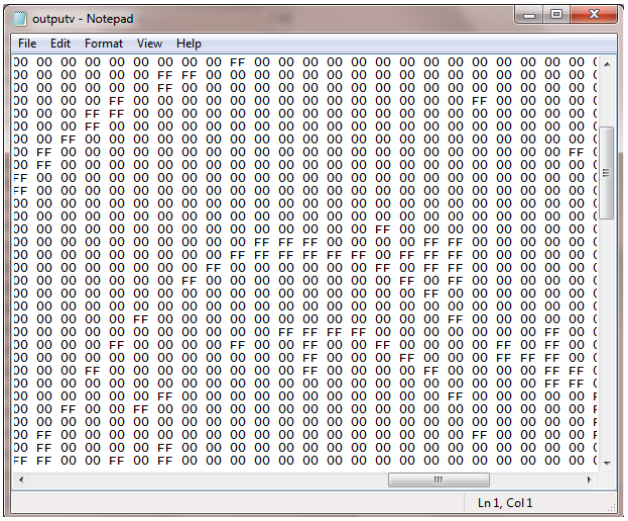

Fig.9 Output Text File of Vertical Edge detected image

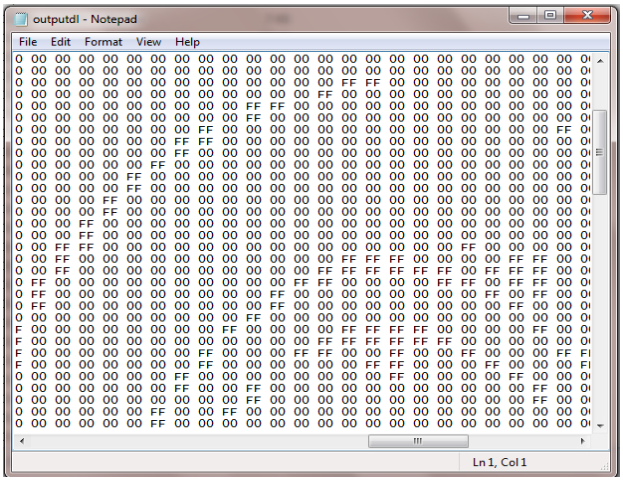

Fig.10 Output Text File of Diagonal Left Edge detected image

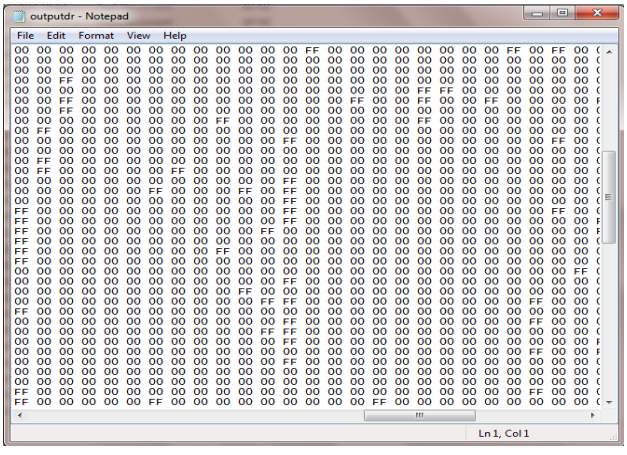

Fig.11 Output Text File of Diagonal Right Edge detected image

The maximum clock frequency is 226.52 MHz on this chip. For providing simulation results the ModelSim and Matlab software are used. Output text file of edge detected image in four directions as shown in figure 8, figure 9, figure 10and figure 11. Gray scale 128×128×8 bits are used as test-bench images for evaluating the proposed processor. The simulation results for Edge detected image are presented in Figure12.

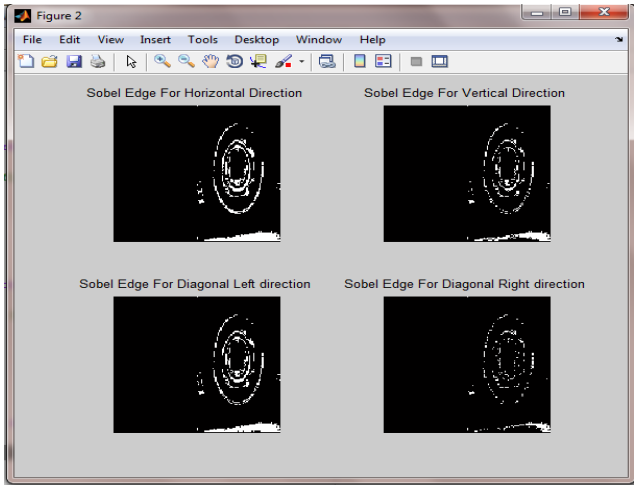

Fig.12 Edge Detected Image

Conclusion

Hardware description of edge detection system based on VHDL was considered of high-speed processing in image edge detection. Hardware architecture of Sobel edge detection algorithm for implementation on field programmable gate array (FPGA) chips was proposed. The proposed architecture calculates the edges of gray scale images in horizontal and vertical direction i.e. (EV, EH) but for more accuracy we can also calculated Edges of gray scale image in diagonal directions i.e. left diagonal and right diagonal (EDL, EDR).Simulation results and synthesizing proposed Sobel edge detection processor on Xilinx Spartan3 XC3S200 FPGA chip demonstrated the efficiency of proposed architecture for edge detecting of gray scale images.

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