Research Article

Design and Implementation of CMOS Temperature Sensor

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Abstract

In this paper we are introducing a temperature sensor based on CMOS design known for its simplicity, reduced parasitic or latch-up and high package density .The paper aims at developing the MOSFET as a temperature sensing element operating in subthreshold region that demands for ability to control the power dissipation. It focuses on temperature measurement using the difference between the gate-source voltages of transistors that is proportional to absolute temperature with low power consumption which facilitates it for low power applications such as battery powered portable devices and in VLSI chips to monitor heat dissipation. This proposed CMOS temperature sensor is able to measure the temperature range from 0^oC to 120^oC . The circuit is designed in concept that utilize on chip CMOS temperature sensor and operates with a single rail power supply of 600mV. The total power consumption of merely is 0.15nW $[0^oC]$ and 12.5nW $[120^oC]$. The sensitivity of the circuit is about 0.12 nW/ ^oC. The layout area of sensor is $81x90\mu m^2$. This circuit is designed & simulated using Cadence Analog & Digital system design tools UMC 180nm technology.

Keywords: CMOS-Complementary Metal Oxide Semiconductor, MOSFET-Metal Oxide Semiconductor Field Effect Transistor ,VLSI-Very Large Scale Integration , Subthreshold, Temperature sensor.

1. Introduction

Temperature is one of the most important fundamental physical quantity and is almost common in our daily life and which is independent of the amount of material i.e. temperature is having intensive property. Nowadays for each & every application new standard circuits are required. As we know hundreds or thousands of devices are formed on thin silicon wafers. Before the wafer is scribed and cut into individual chips, they are usually laser trimmed. One popular use of embedded temperature sensors in VLSI implementation is in the emergence of RFID and wireless sensor network (WSN) applications. For deployment in such applications, power consumption, instead of sensing range and accuracy requirements, is of utmost importance. Process compensated CMOS temperature sensor (Yaesuk et al, 2012) has designed for microprocessor application. The beauty of this circuit is no need of any BJT component.One of the popular method (Pertijs et al, 2004) is by using the difference between the base-emitter voltages of a substrate PNP transistor (thermal diode), which is fed by two different currents (Tuthill M. et al,1998). These sensors in general achieve good accuracy, with the penalties of increased circuit complexity and power dissipation(Pertijs et al, 2005). The temperature sensors have been realized using a time-to-digital-converter, or a ring-oscillator, in a 0.35 µm

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process or below. However, such temperature sensors consume power at the required sampling rate (Chen, P et al, 2005).

Temperature is a physical quantity that is a measure of hotness and coldness on a numerical scale(Maxwell, J.C. et al, 1871). In a body in its own internal thermal equilibrium, the temperature is spatially uniform. Temperature is important in all fields of natural science.

As we know ICs designed chips from BJT are good in some operational conditions but there are problems of power dissipation and package density. In the past few years ,along with advance in CMOS technology ,more and more components are integrated in a chip (D Patranabis et al , 2008). In CMOS circuit NMOS transistor are used as the best driver and PMOS as a load. Decreasing feature size and increasing package density cause self-heating of chips to become an important factor. Hence to reduce the latch-up/parasitic effect we intend to utilize CMOS SOI technology for the same purpose. With the help of on-chip temperature sensors, we could avoid thermal damage and increase reliability via thermal monitoring system.Since by decreasing the gate length the latch-up/parasitic effect increases.

In this paper, I want to present a microWatt integrated temperature sensor for ultra-low power applications designed and simulated using Cadence analog and digital system design tools UMC 180nm CMOS technology. Ultra-low power consumption is achieved through the use of sub-threshold (also known as weak inversion) MOS operation. The transistor are used in this domain because

the current here is exponentially dependent on the control voltages of the MOSFET and they draw small currents so as to reduce power consumption. The sensor sinks current in nano-amperes say around 10-20 nA from a single power supply of 0.6V and its power consumption is around 12.5nW. The performance of the sensor is highly linear in the range of 0–120 ^{0}C.

2. Proposed Scheme

This paper proposes the block diagram as shown in figure 1 of a temperature sensor which consists of:
(i) Current source sub-circuit
(ii) Temperature variable sub-circuit
(iii) One point caliberation sub-circuit

(i) Current source sub-circuit:
It is a self-biasing circuit that generates a current independent of voltage source.
(ii) Temperature variable sub-circuit:
It accepts current through PMOS current mirrors and produces an output voltage proportional to temperature. The temperature variable sub-circuit consists of three couples of serially connected transistors operating in subthreshold region where the drain current and the gate-source voltage of a MOSFET show an exponential relationship.
(iii) One point caliberation sub-circuit:
After packaging, the sensor is calibrated by measuring its die temperature at reference point using on-chip calibration transistors.
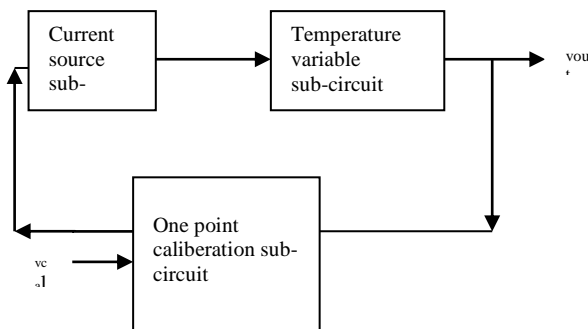

Fig.1 Block diagram of a temperature sensor

3. Methodology

The sub-threshold drain current I_D of a MOSFET is an exponential function of the gate-source voltage V_{GS} and the drain source voltage V_{DS}, and given by:

$$I_D = KI_0 exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \times 1 - exp\left(\frac{-V_{DS}}{V_T}\right), \quad (1)$$

Where
$$I_0 = \mu C_{OX}(\eta - 1) \times V_T^2, \quad (2)$$

and K is the aspect ratio (=W/L) of the transistor, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, V_T is the thermal voltage V_{TH} is the threshold voltage of a MOSFET, and η is the sub-threshold slope factor.

In the current-source sub-circuit, gate-source voltage V_{GS9} is equal to the sum of gate-source voltage V_{GS8} and drain

source voltage V_{DS10} (Ali Sahafi et al, 2013):

$$V_{GS9} = V_{DS10} + V_{GS8} \quad (3)$$
$$V_{DS10} = V_{GS9} - V_{GS8} = \eta V_T In\left(\frac{K_8}{K_9}\right) \quad (4)$$

M_{10} is operated in the sub-threshold region, so transconductance G_{DS10} is obtained by using Eqs. (1) and (4) :

$$G_{DS10} = \frac{\partial I_{DS10}}{\partial V_{DS10}} = \frac{K_{10}I_0}{V_T}exp\left(\frac{V_m-V_{TH10}}{\eta V_T} - \frac{V_{DS10}}{V_T}\right) \quad (5)$$
$$I = V_{DS10} \times G_{DS10}$$
$$= \eta K_1 I_0 \left(\frac{K_9}{K_8}\right)^{\eta} \left(In\left(\frac{K_8}{K_9}\right)\right) exp\left(\frac{V_m-V_{TH10}}{\eta V_T}\right) \quad (6)$$

As M_{10} operates in sub-threshold region (V_m - V_{TH10}<0), I is increased by temperature, so the highest power consumption is in the upper temperature limit and the maximum current can be limited by size of the transistors. Choosing the maximum current is a tradeoff between power consumption and linearity that can be obtained by simulation.

In the temperature variable sub-circuit, as M_5, M_6, M_{15}, M_{12}, M_{16},M_{17} are in sub-threshold region, the relation between gate to source voltage and MOS current is equal to Eq. (4). According to Fig. 2, currents of M_5, M_{12}, M_{16}, M_{17} are I and currents of M_6 and M_{15} are 3I and 2I respectively also shown in Figure 6.

$$V_{OUT} = V_{GS6} - V_{GS5} + V_{GS15} - V_{GS12} + V_{GS16} - V_{GS17} \quad (7)$$

By using Eq. (4) with regard to currents of MOSFETs, output voltage is given by:

$$V_{OUT} = \eta V_T In\left(\frac{I_{D6}I_{D15}I_{D16}K_5K_{12}K_{17}}{I_{D5}I_{D12}I_{D17}K_6K_{15}K_{16}}\right) + \Delta V_{TH} \quad (8)$$

By replacing the currents of transistors, output voltage is obtained by:

$$V_{OUT} = \eta V_T In\left(\frac{6K_5K_{12}K_{17}}{K_6K_{15}K_{16}}\right) + \Delta V_{TH} \quad (9)$$

By combination of Eqs. (7) and (9) output voltage can be obtained:

$$V_{OUT} = \frac{\eta K_B T}{q} In\left(\frac{6K_5K_{12}K_{17}}{K_6K_{15}K_{16}}\right) + \Delta V_{TH0} = A \times T + B \quad (10)$$

where T is absolute temperature, A and B are temperature independent constants. Eq. (10) shows a linear relationship between absolute temperature and output voltage.

4. Simulation Result & Discussion

4.1. Selection of Temperature Range

We plotted the graph between output Voltage and drain current with respect to Temperature as shown in Figure 3. In simulation we achieved wider excellent linearity between the ranges 0°C to 120°C and the voltage difference between this two temperature ranges is also good at power supply voltage V_{DD}=600mV.
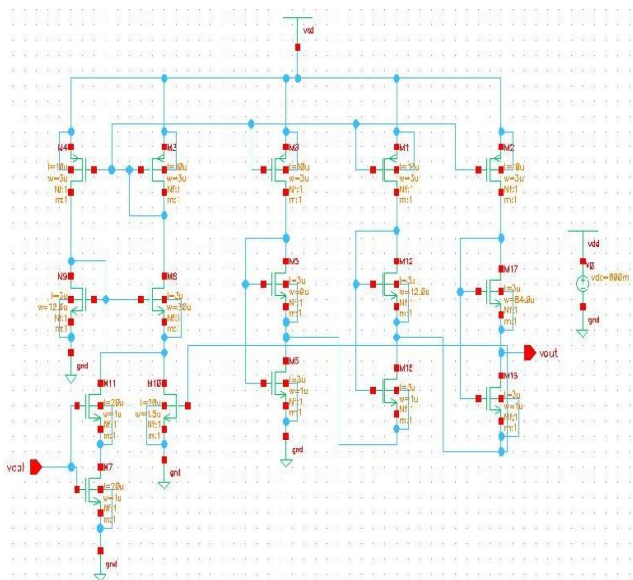
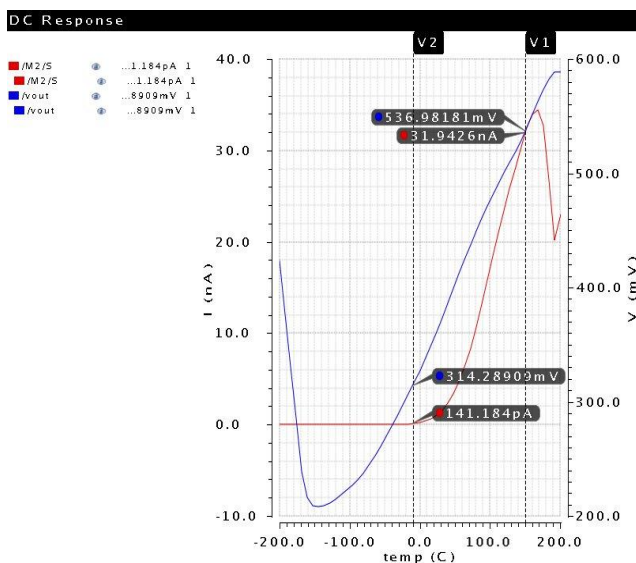**Fig 2**. Circuit diagram of CMOS temperature sensor

Fig 3. Voltage and current versus Temperature graph for Selection of suitable Temperature Range
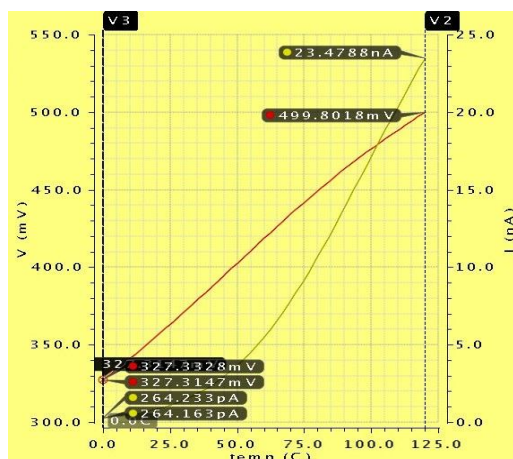

Fig 4. Voltage and Sink current versus Temperature graph

4.2. *Voltage and Sink current versus Temperature graph*

We plotted a graph between the voltage and sink current drawn from the power supply of 600mV for different range of temperature as shown in Figure 4.
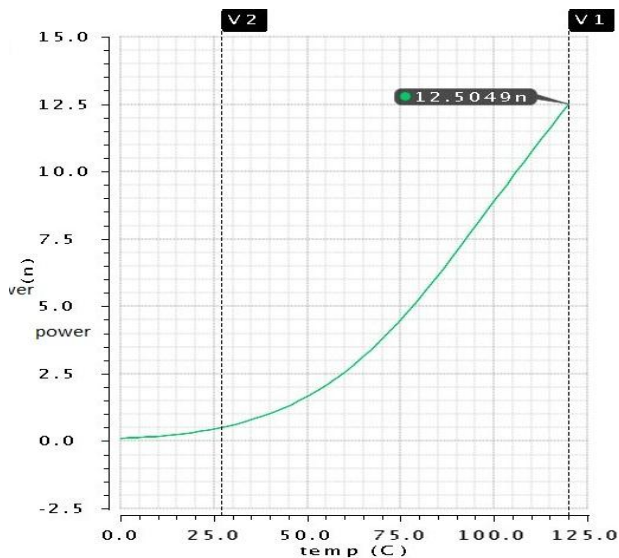

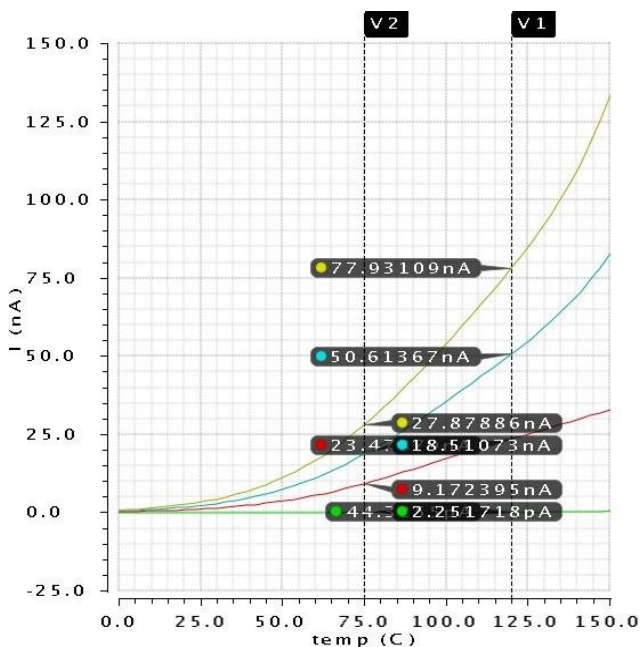**Fig 5**. Power versus Temperature graph.

Fig 6. Current relation graph of different MOSFETS as of M_5, M_{12}, M_{16}, M_{17}(red dot) are I and currents of M_6(yellow dot) and M_{15}(blue dot) are 3I and 2I respectively.

Table 1 Performance Summary

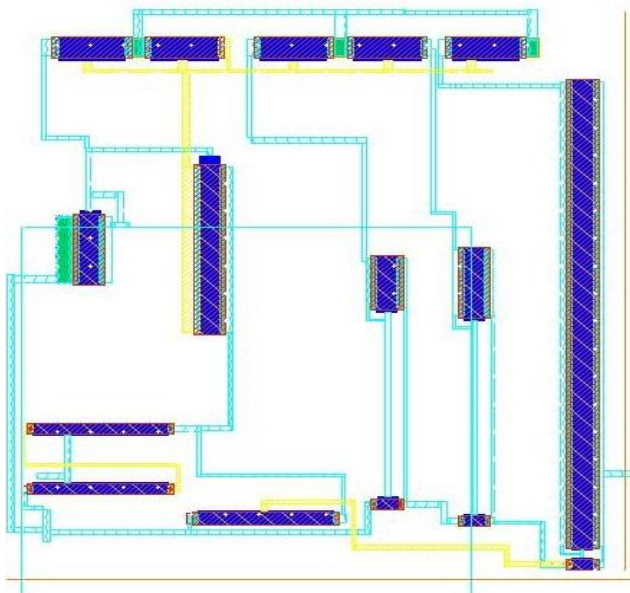| Parameter	Value
Power Supply	600mV
Power Consumption	12.5 nW @ 120°C
Circuit Area	0.0073mm^2
Sensitivity	0.12nW/^{o}C

Fig 7. Layout of CMOS temperature sensor

4.3. Power calculation at different Temperature ranges for fixed power supply

The power is calculated at different temperature ranges from 0^oC to 120^oC with a fixed power supply of 600mV is shown in Table 2 and in Figure 5.

Table 2 Power at different Temperature range

Temperature in Centigrade	POWER in Nanowatt
0^oC	0.15nW
25^oC	0.5nW
120^oC	12.5nW

Conclusions

The main focus is to design a highly linear ultra low power CMOS temperature sensor to enhance the measurement accuracy while applying to the on-chip thermal monitoring of VLSI chips and in low powered communication devices The sensor should be featured with a small or low power consumption of merely 12.5 nW at 120 ˚C and 0.5 nW at room temperature. The sensor is designed and simulated by Cadence Spectre software in the 0.18um CMOS technology process with supply voltage of 600m V.

References

Yaesuk Jeong and Farrokh Ayazi(2012) Process Compensated CMOS Temperature   Sensors for Microprocessor Applications *IEEE Journal* 2012.

Intel Pentium D Processor 900 Sequence and Intel Pentium Processor Extreme Edition 955 Datasheet,(2006). On 65 nm Process in the 775-Land LGA Package and Supporting Intel Extended Memory 64 Technology, and Supporting Intel Virtualization Technology, Intel Corp., Document 310306-002.

AMD Functional Data Sheet, 940 Pin Package, Advanced Micro Devices, Inc., 31412, Rev 3.05 (2004).

IBM PowerPC 970FX RISC Microprocessor Data Sheet IBM Corp.(2005) Preliminary Electrical Information, SA14-2760-05, Version 2.1.

Pertijs, M. A. P., Meijer, G. C. M., & Huijsing, J. H. (2004). Precision temperature measurement using CMOS substrate pnptransistors. *IEEE Sensors Journal*, 4(3), 294–300.

Tuthill M. (1998) A switched-current, switched-capacitor temperature sensor in 0.6 µm CMOS. *IEEE Journal of Solid-State Circuits*, 33(7), 1117–1122.

Pertijs, M. A. P., Niederkorn, A., Xu, M., McKillop, B., Bakker, A., & Huijsing, J. H. (2005). A CMOS smart temperature sensor with a 3σ inaccuracy of 0.5 ˚C from -50 to 120 ˚C. *IEEE Journal of Solid-State Circuits*, 40(2), 454–461.

 Chen, P., Chen, C. C., Tsai, C. C., & Lu, W. F. (2005) time-todigital-converter-based CMOS smart temperature sensor. *IEEE Journal of Solid-State Circuits* , 40(8), 1642–1648.

Maxwell, J.C.(1871) Theory of Heat, Longmans, Green, and Co., London.pp.2-6,1871.

D Patranabis, Sensors and Transducers(2008) Text book, Prentice-Hall of India Private limited, New Delhi pp.103-108.

Ali Sahafi, Jafar Sobhi, Ziaddin Daie Koozehkanani(2013),Nanowatt CMOS temperature sensor, *Springer Analog Integr circ sig process* 75:343-348 .