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Research Article

Voltage Scaling Based Energy Efficient FIR Filter Design on FPGA

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Abstract

In this paper Voltage Scaling is used to design energy efficient Gaussian FIR Filter. This design is implemented on Kintex-7 FPGA, XC7K70T device, -3 speed grade and FBG676 package. Among all powers in FPGA, it is observed that Logic Power have maximum Power reduction of 100% at 5GHz and IO power have minimum power reduction of 2.25% at 1 THz, while the voltage is scaled from 1.0 to 0.2V. Clock power is reduced up to 86.11%, 87.14%, 87.10% and 87.26% and Leakage power is reduced to up to 50.39%, 66%, 82.78% and 82.78%, when the FIR filter is operated at 5GHz, 50GHz, 500GHz and 1 THz frequencies respectively and voltage is scaled down from 1.0V to 0.2V.

Keywords: *Voltage Scaling, FIR Filter, Energy Efficient Design, FPGA, Power Dissipation*

1. Introduction

Digital filters works in the domain of time sequence and that takes a sequence of fixed length, discrete input and generates output sequence.

Figure 1: Finite Impulse Response (FIR) Filter

A finite duration impulse response (FIR) filter generates its output as a weighted sum of its present values and past input values as shown in Figure 1. In Digital Signal processing, it is important to have power optimized digital filters, for that reason, we are using voltage scaling approach. We are scaling voltage values from 1.0V to 0.2V with step size of 0.2. We are using four frequencies of 5GHZ, 50GHz, 500GHz and 1THz and examining the power consumption in Finite Duration Impulse Response (FIR) Filter.

1. 1Literature Review

Some work provides the information about effect of buses on to stability of steady state voltage. Some suggested based on normal forms of diffeomorphism, equation of power flow is observed and concept of nonlinearity is also considered for power system. Features of battery discharge are observed and discover that entire discharge of battery takes a nonlinear and linear discharge step.Some work shows some of the problems and features dynamic voltage/frequency scaling in data centres. The important procedure to get high velocity and accurate FPGA and provides efficient FIR filter design of serial shift and it avoids the limitation old parallel algorithm which take huge amount of hardware resources. Few people tells about implementation of window function based FIR filter and implemented on chip TMS320C5410.

2. RTL Schematic Diagram of FIR FILTER

Figure 2, shows the Register Transfer Level (RTL) schematic diagram of Finite Duration Impulse Response (FIR). There are two 8x3-to-18-bit MAC, three 8x6-to-18-bit MAC and two 8x5-to-18-bit MAC. There are 64 flip flops and one 18 bit/2-input adder tree as shown in Figure 2.

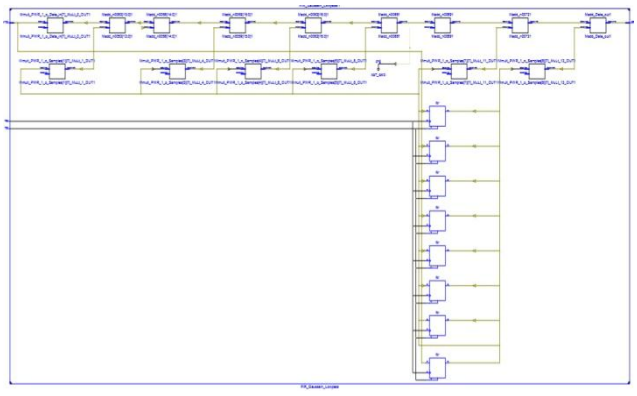

Figure 2: RTL Schematic Diagram of FIR Filter

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3. Power Dissipation Using Voltage Scaling

In order to make FIR filter more efficient, we are using voltage scaling approach. We are scaling voltage values from 1.0V to 0.8V, 0.6V, 0.4V and 0.2V. Using four frequencies we are analysing the power dissipation in Finite Duration Impulse Response (FIR) Filter.

3.1. Clock Power Dissipation at Different frequencies

Table 1: Clock Power Dissipation at Different Frequencies

Power→ Frequency↓	1.0V	0.8V	0.6V	0.4V	0.2V
5GHz	0.036	0.026	0.018	0.010	0.005
50GHz	0.350	0.255	0.173	0.103	0.045
500GHz	3.505	2.555	1.729	1.028	0.452
1THz	7.169	5.215	3.521	2.087	0.913

As the voltage of the device decreases, its clock power also decreases. Table 1 shows clock power at different frequencies. At 5GHz frequency the clock power is 0.036w, 0.026W, 0.018W, 0.005W, when the voltage of the target circuit is kept at 1.0V, 0.8V, 0.6V, 0.4V and 0.2V respectively.

3.2. Logic Power Dissipation at Different frequencies

Table 2: Logic Power Dissipation at Different Frequencies

Power→ Frequency↓	1.0V	0.8V	0.6V	0.4V	0.2V
5GHz	0.002	0.002	0.001	0.000	0.000
50GHz	0.016	0.010	0.006	0.003	0.001
500GHz	0.751	0.091	0.051	0.023	0.006
1THz	0.281	0.180	0.101	0.045	0.011

In Table 2, Logic power of the circuit becomes 0.016W, 0.010W, 0.006W, 0.003W, 0.001W at voltages 1.0V, 0.8V, 0.6V, 0.4V and 0.2V respectively and device operating frequency is 5GHz.

3.3. Signal Power Dissipation at Different frequencies

Table 3: Signal Power Dissipation at Different Frequencies

Power→ Frequency↓	1.0V	0.8V	0.6V	0.4V	0.2V
5GHz	0.019	0.015	0.008	0.004	0.001
50GHz	0.179	0.114	0.064	0.029	0.007
500GHz	1.320	1.102	0.620	0.276	0.069
1THz	3.424	2.192	1.233	0.548	0.137

In Table 3, When the FIR is operating at 500GHz and voltage values are 1.0V, 0.8V, 0.6V, 0.4V and 0.2V Signal power becomes 1.320W, 1.102W, 0.620W, 0.276W and 0.069W respectively.

3.4. DSPs Power Dissipation at Different frequencies

Table 4: DSPs Power Dissipation at Different Frequencies

Power→ Frequency↓	1.0V	0.8V	0.6V	0.4V	0.2V
5GHz	0.104	0.078	0.044	0.020	0.005
50GHz	1.219	0.780	0.439	0.195	0.049
500GHz	10.358	7.803	4.389	1.951	0.488
1THz	24.386	15.607	8.779	3.902	0.975

In Table 4, we are getting significant amount of reduction in DSPs power. AT 5GHz and when the voltage is scaled down to 0.2V, there is 95.19% reduction in DSPs power.

3.5. IO Power Dissipation at Different frequencies

Table 5: IO Power Dissipation at Different Frequencies

Power→ Frequency↓	1.0V	0.8V	0.6V	0.4V	0.2V
5GHz	0.83	0.747	0.742	0.738	0.734
50GHz	7.51	7.468	7.425	7.382	7.339
500GHz	81.1	74.68	74.24	1.951	73.39
1THz	150.2	149.36	148.49	147.636	146.7

There is very less reduction in IO power as compared to other powers. IO power is reduced up to 9.61% at 500GHz, when the voltage is scaled from 1.0V to 0.2V as shown in Table 5.

3.6. Leakage Power Dissipation at Different frequencies

Table 6: Leakage Power Dissipation at Different Frequencies

Power→ Frequency↓	1.0V	0.8V	0.6V	0.4V	0.2V
5GHz	0.127	0.093	0.076	0.067	0.063
50GHz	0.203	0.129	0.093	0.077	0.069
500GHz	1.028	0.575	0.344	0.230	0.177
1THz	1.028	0.571	0.344	0.230	0.177

Leakage power is also termed as static power in FPGA. We are achieving maximum of 82.78% less reduction in Leakage power at 500GHz and 1THz when voltage is scaled down up to 0.2V as shown in Table 6.

3.7. Comparison of Power Dissipation at 5GHz

Table 7: Comparison of Power Dissipation at 5GHz

Voltage→ Power↓	1.0V	0.8V	0.6V	0.4V	0.2V
Clock	0.036	0.026	0.018	0.010	0.005
Logic	0.002	0.002	0.001	0.000	0.000
Signal	0.019	0.015	0.008	0.004	0.001
DSPs	0.104	0.078	0.044	0.020	0.005
IO	0.751	0.747	0.742	0.738	0.734
Leakage	0.127	0.093	0.076	0.067	0.063

Table 7 and Figure 3, shows the comparison of different powers at different voltages at 5GHz. When we are scaling down voltage of device from 1.0V to 0.2V, we are getting 86.11%, 100%, 94.73%, 95.19%, 2.26% and 50.39% less reduction in Clock power, Logic Power, Signal power, DSPs power, IO power and Leakage power respectively.

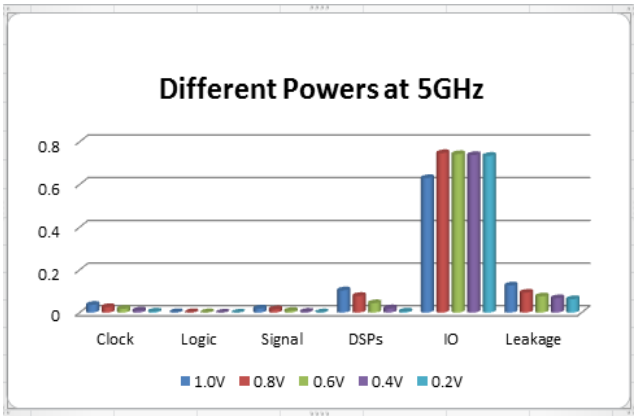

Figure 3: Comparison of Power Dissipation at 5GHz

3.8. Comparison of Power Dissipation at 50GHz

Table 8: Comparison of Power Dissipation at 50GHz

Voltage→ Power↓	1.0V	0.8V	0.6V	0.4V	0.2V
Clock	0.350	0.255	0.173	0.103	0.045
Logic	0.016	0.010	0.006	0.003	0.001
Signal	0.179	0.114	0.064	0.029	0.007
DSPs	1.219	0.780	0.439	0.195	0.049
IO	7.511	7.468	7.425	7.382	7.339
Leakage	0.203	0.129	0.093	0.077	0.069

In Table 8 and Figure 4, at 50 GHz operating frequency, the reduction in Clock power, Logic Power, Signal power, DSPs power, IO power and Leakage power become 287.14%, 93.75%, 96.08%, 95.98%, 2.28% and 66% respectively, when the voltage is scaled from 1.0V to 0.2V.

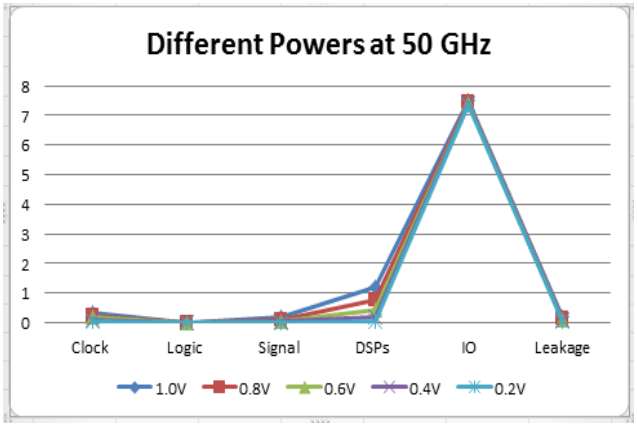

Figure 4: Comparison of Power Dissipation at 50GHz

3.9 Comparison of Power Dissipation at 500GHz

Table 9: Comparison of Power Dissipation at 500GHz

Voltage→ Power↓	1.0V	0.8V	0.6V	0.4V	0.2V
Clock	3.505	2.555	1.729	1.028	0.452
Logic	0.087	0.091	0.051	0.023	0.006
Signal	1.320	1.102	0.620	0.276	0.069
DSPs	10.358	7.803	4.389	1.951	0.488
IO	81.193	74.680	74.249	1.951	73.39
Leakage	1.028	0.575	0.344	0.230	0.177

By the scaling the voltage from 1.0V to 0.2V, clock power and Logic power is reduce to 87.10% and 93.10% respectively, when the FIR is operated at 500GHz frequency as shown in Table 9 and Figure 5.

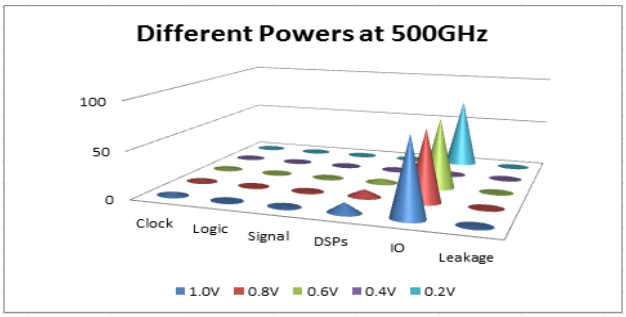

Figure 5: Comparison of Power Dissipation at 500GHz

3.10 Comparison of Power Dissipation at 1THz

Table 10: Comparison of Power Dissipation at 1THz

Voltage→ Power↓	1.0V	0.8V	0.6V	0.4V	0.2V
Clock	7.169	5.215	3.521	2.087	0.913
Logic	0.281	0.180	0.101	0.045	0.011
Signal	3.424	2.192	1.233	0.548	0.137
DSPs	24.3	15.60	8.779	3.902	0.975
IO	150.2	149.36	148.499	147.636	146.7
Leakage	1.02	0.571	0.344	0.230	0.177

On operating the FIR at 1THz frequency and scaling the voltage from 1.0V to 0.2V, there is 96% and 82.78% less reduction in DSPs power and Leakage power respectively as shown in Table 10 and Figure 4.

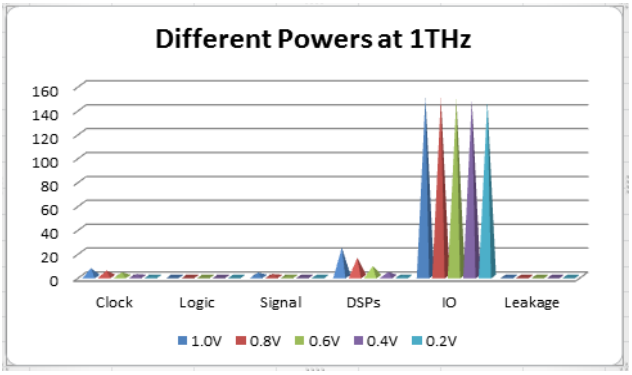

Figure 6: Comparison of Power Dissipation at 1THz

Conclusion

In Digital Signal processing, FIR filter is considered an important filter. On operating the FIR at 5GHz frequency and scaling the voltage from 1.0V to 0.2V, Clock power, Logic Power, Signal power, DSPs power, IO power and Leakage power is reduced up to 86.11%, 100%, 94.73%, 95.19%, 2.26% and 50.39 respectively. There is 87.26%, 96.08%, 95.99%, 96%, 2.29% and 82.78% less IO reduction in Clock power, Logic Power, Signal power, DSPs power, IO power and Leakage power respectively. It is observed that we are getting maximum reduction in Logic power at 5GHz and minimum reduction in IO power at 1 THz, when the voltage is scaled from 1.0V to 0.2V.

Future Scope

Kintex-7 FPGA is used to implement this FIR Gaussian Filter. Airtex-7 can also be used in future for implementing this FIR Filter. Voltage Scaling is considered to be one of good approach for reduction in power in Digital Signal Processing. There is a wide scope to apply this voltage Scaling technique to different Filters of DSPs, in order to make them energy efficient.

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