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Research Article

Energy Conversion in 64-Bit ALU Design on FPGA Using Mechanics of Capacitance

Sweety[À], Tanesh Kumar[Ḃ*], B Pandey[Ḃ], S.M M Islam[Ḃ] and Teerath Das[Ḃ]

[À] aharaja Surajmal Institute, Delhi, India
[Ḃ] South Asian University, New Delhi, India

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Abstract

In this paper an energy conversion in 64-bit Arithmetic Logic Unit (ALU) design is analyzed using an approach termed as Capacitance Mechanics. It is observed that when the Arithmetic Logic Unit is operated at frequencies of 1GHz, 10GHz, 100GHz and 1THz, total power is reduced to 52.70%, 65.28%, 67.60% and 67.85% respectively, when we are scaling down the capacitance from 50pF to 0pF. This ALU design is implemented on XC6VLX75T device Virtex-6 FPGA with -2 speed grade and FF484 package.

Keywords: *Arithmetic Logic Unit (ALU), Capacitance Mechanics, Energy Conversion, FPGA, Power Mechanics*

1. Introduction

Arithmetic Logic Unit (ALU) is an important part of Central processing Unit (CPU) and performs Logical and Arithmetic operations on Data. Registers, Memory, Control Unit are the other components of a computer system, which are used to support ALU by taking data as an input in ALU for processing purpose. After ALU processing phase, data is again taken back out by these supporting components. Figure 1 shows the interconnection of ALU with other components of the processor.

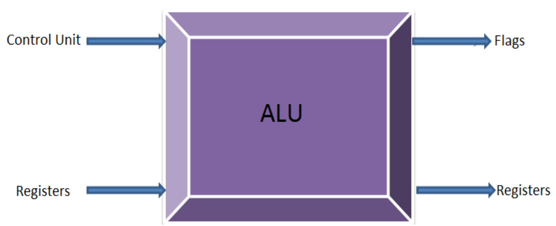

Figure 1: ALU Inputs and Outputs

Data is given to ALU in registers and after performing some operations on data, the result is again stored in registers. A set flag can also be set by ALU, as result of some operation. We have taken 64-bit ALU as our target circuit for this paper. In electronics, capacitance scaling is a widely used technique to reduce the power of electronic devices.

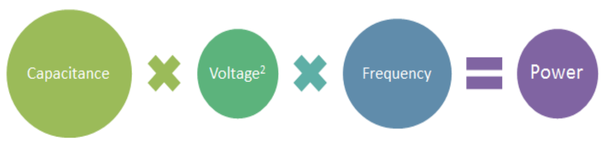

Figure 2: Mathematical Expression for Power and Capacitance

In order to make 64-bit ALU energy efficient, we are applying capacitance scaling technique to our target circuit. Power is directly proportional to capacitance and frequency as shown in Figure 2.

Related Work

Clock gating, Word-length Optimization, pipelining and Dynamic Voltage Scaling are the some basic techniques of low energy approaches for field programmable Gate Array is mentioned by some authors, their work gave information about Urdhva Triyagbhyam– Vedic Multiplication approach and it allows generation of intermediate products in parallel, removes undesirable steps of multiplication with zeros and at higher bit levels it is scaled using Karatsuba algorithm. For the purpose of reduction in dynamic power requirements of 8-bit Arithmetic Logic Unit (ALU), clock gating approach is used. When we add clock gate to out target circuit and is operating at frequencies of 1GHz-1THz, Clock power reduced to there is17.85%, 23.39%, 26.49% and 27.19% reduction in clock power of the total dynamic power mentioned by some authors low power 16-bit ALU is designed and carry skip adder is used with variable block length, to get better performance. By repositioning

*Corresponding author: Tanesh Kumar

functional elements in the chain, a chain-structure based Arithmetic Logic Unit is designed . Power saving achieved in range from 43.5% to 49.6% and most importantly this result is achieved without any risk of processor performance and hardware complexity. For high speed and low power ALU an approach termed as Feedback-Switch Logic (FSL) is used. Using static complementary metal oxide semiconductor (CMOS) and logics of Feedback-Switch Logic (FSL) at 90nm CMOS process, a 32-bit Arithmetic Logic Unit (ALU) is designed and this ALU is low energy and high performance. Result after simulation tells that they achieved delay reduction by 14% at the sake of increment of 8% energy dissipation in comparison with static logic of the CMOS.

Operations of ALU

Many different types of operations is performed by Arithmetic Logic Unit (ALU), i.e. Arithmetic Operation and Logic Operations. Arithmetic operations includes operations like Addition, Subtraction, Multiplication, Division, while Logic operations includes operations like AND, OR and NOT. Operations like shift and rotate are also performed in ALU..

1.1. Arithmetic operations of ALU

Arithmetic operation in Arithmetic Logic Unit includes operations like addition, subtraction, multiplication and division.

1.1.1. Addition Operation of ALU

Figure 3 shows the Addition operations of ALU. If we have value of Input1 equal to 18 and input2 value equal to 15, then after addition, output will be 33.

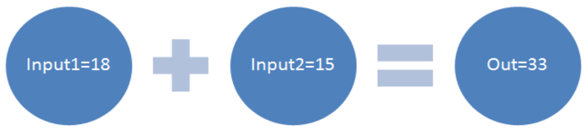

Figure 3: Addition Operation of ALU

1.1.2. Subtraction Operation in ALU

If we have Input1 equals to 35 and Input2 equals to 13, then after subtraction operation in ALU, the result will be 22 as shown in Figure 4.

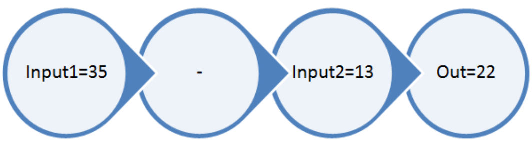

Figure 4: Subtraction Operation of ALU

1.1.3. Multiplication Operations of ALU

In Figure 5, When the Input1 is 3 and Input2 is 4, so output of multiplication operation of ALU will be 12.

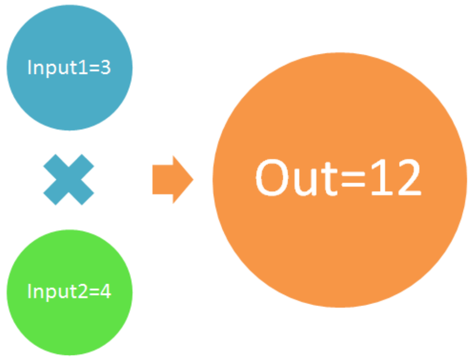

Figure 5: Multiplication Operation of ALU

1.1.4. Division Operation of ALU

In Figure 6, for the division operation of ALU output will come 4, if the Input1 and Input2 values are equal to 24 and 6 respectively.

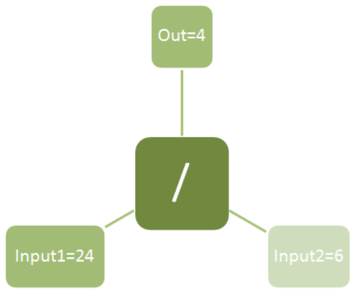

Figure 6: Division Operation of ALU

1.2. Logical Operations OF ALU

Logical Operation in Arithmetic Logic Unit includes Logical operations like AND, OR, and NOT.

1.2.1. AND Operation of ALU

AND is the Logical Operation of the ALU. In Figure 7, Input1 is equal to 0 0 1 1 and Input2 is equal to 0 1 0 1. After AND operation the output will be 0 0 0 1.

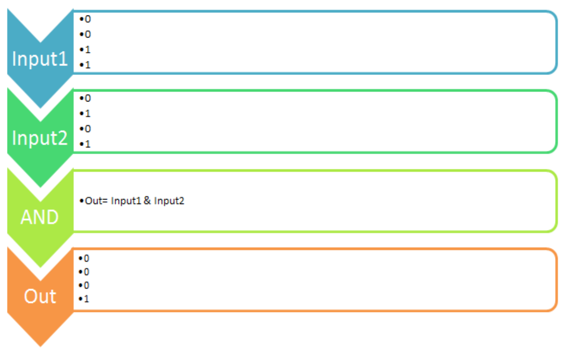

Figure 7: AND Operation of ALU

1.2.2. OR Operation of ALU

From Figure 8, after applying OR operations, the result will be 0 1 1 1, if the Input1 is 0 0 1 1 and Input2 is 0 1 0 1.

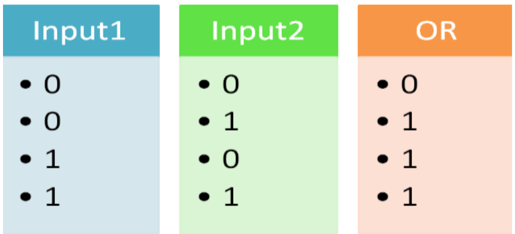

Figure 8: OR Operation of ALU

1.2.3. NOT Operation of ALU

NOT operation is process of inverting every input bit of data. If the input is 0 after NOT operation the output will be 1 and if the input is 1, the output will be 0 after NOT operation. In Figure 9 Input is 0 1 and after applying NOT operation output becomes 1 0.

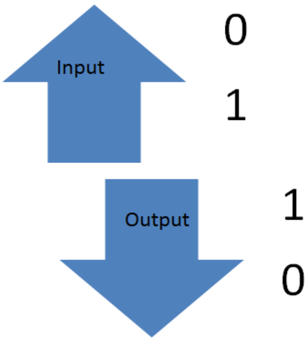

Figure 9: NOT Operation of ALU

2. Capacitance Scaling

In Capacitance Scaling we are scaling the capacitance value from 50pF to 40pF, 30pF, 20pF, 10pF and 0pF under different frequencies and analysing the power consumption.

2.1. Total Power Consumption at 50pF

Table 1: Total Power Consumption at 50pF

	Total Power
1GHz	5.941
10GHz	46.875
100GHz	452.328
1THz	4506.583

With the increase of frequency, total power of 64-bit ALU is also increases. In table 1, Total power is 5.941W, 46.875W, 452.328W and 4506.583W at 1GHz, 10GHz, 100GHz and 1THz respectively.

2.2. Total Power Consumption at40pF

Table 2: Total Power Consumption at 40pF

	Total Power
1GHz	5.316
10GHz	40.760
100GHz	391.172
1THz	3895.024

As we decrease the capacitance of 64-bit ALU, its power is also decrease. In table 2, when 64-bit ALU is operated at 1GHz, 10GHz, 100GHz and 1THz device operating frequencies, the total power becomes 5.316W, 40.760W, 391.172W and 3895.024Wrespectively.

2.3. Total Power Consumption at 30pF

Table 3: Total Power Consumption at 30pF

	Total Power
1GHz	4.689
10GHz	34.644
100GHz	330.016
1THz	3283.464

In Table 3, at 30pF capacitance, total power is 4.689W, 34.644W, 330.016W and 3283.464W, when the Arithmetic Logic Unit is operating at 1GHz, 10GHz, 100GHz and 1THz frequencies.

2.4. Total Power Consumption at 20pF

Table 4: Total Power Consumption at 20pF

	Total Power
1GHz	4.062
10GHz	28.528
100GHz	268.866
1THz	2671.905

In Table 4, when 64-bit ALU is operated at device frequencies 1GHz, 10GHz, 100GHz and 1THz the total power of the target circuit becomes 4.062W, 28.528W, 268.866W and 2671.905W respectively.

2.5. Total Power Consumption at 10pF

Table 5: Total Power Consumption at 10pF

	Total Power
1GHz	3.436
10GHz	22.395
100GHz	207.704
1THz	2060.346

In Table 5, total power is 3.436W, 22.395W, 207.704W and 2060.346W on device operating frequencies 1GHz, 10GHz, 100GHz and 1THz respectively.

2.6. Total Power Consumption at 0pF

Table 6: Total Power Consumption at 0pF

	Total Power
1GHz	2.810
10GHz	16.271
100GHz	146.548
1THz	1448.786

In Table 6, when capacitance value is taken as 0pF, and device operating frequencies is taken as 1GHz, 10GHz, 100GHz and 1THz total power becomes 2.810W, 16.271W, 146.548W and 1448.786W respectively.

2.7. Comparison of Total power at Different Frequencies

Table 7: Total Power Comparison at different Frequencies

Capacitance→ Frequency↓	50pF	30pF	10pF	0pF
1GHz	5.941	4.689	3.436	2.810
10GHZ	46.875	34.644	22.395	16.271
100GHz	452.32	330.0	207.704	146.548
1THz	4506.5	3283.4	2060.346	1448.786

Table 7 and Figure 10, at different Capacitance values and under different device operating frequencies, we are comparing total power of 64-bit Arithmetic Logic Unit. From analysis, it is found that, when we are scaling the capacitance from 50pF to 0pF, we are getting 52.70%, 65.28%, 67.60% and 67.85% less reduction in total power, when the 64-bit Arithmetic Logic Unit is operated at operating frequencies of 1GHz, 10GHz, 100GHz and 1THz respectively. .

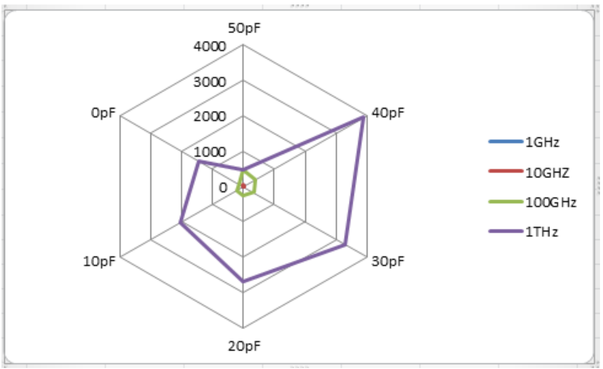

Figure 10: Total Power Comparison at Different Capacitance under different frequencies

Conclusion

Our main aim is to design a power optimized 64-bit Arithmetic Logic Unit (ALU), and for that reason we are using capacitance scaling technique. When we are scaling the capacitance from 50 pF to 0pF, and operating the ALU with 1GHz, 10GHz, 100GHz and 1THz frequencies, then total power is reduced by 52.70%, 65.28%, 67.60% and 67.85% respectively. For this 64-bit ALU design we took Xilinx ISE 14.6 as simulator.

Future Scope

Virtex-6 FPGA is used for implementing this Arithmetic Logic Unit (ALU) design. There is huge possibility to redesign this 64-bit Arithmetic Logic Unit (ALU) on Virtex-7 and Airtex-7 FPGA. Using same framework, there is a good scope to design 128-bit ALU and even 256-bit ALU.

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