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Research Article

Electrical characteristics and performance comparison between partially-depleted SOI and n-MOS Devices using Silvaco T-CAD Simulator

Gautam Kumar Jaiswal[Ȧ*], Anil Kumar[Ȧ], A.K.Jaiswal[Ȧ], Rajeev Paulus[Ȧ] and Mayur Kumar[Ȧ]

[Ȧ]ECE Department/ SHIATS-DU,Allahabad, U.P. INDIA

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Abstract

Electrical characteristics performance comparison between partially-depleted SOI and n-MOS Devices in order to compare their electrical characteristics using Silvaco software is done and presented in this paper.One specific channel lengths of the Device that had been concentrated as 0.4 micron. The comparisons were focused on three main electrical characteristics that are leakage current, threshold voltage and subthreshold voltage. The device structures were constructed using Silvaco-Athena and the characteristics were examined and simulated using Silvaco-Atlas. Results were analysed and presented to show that the electrical characteristics of partially-depleted SOI devices are better than that of bulk-Si devices. It has also shown that the partially depleted SOI device is superior in the submicron region.

Keywords: *NMOS, SILVACO, ATHENA, ATLAS, SOI, PDSOI, FDSOI, DTMOS*

1. Introduction

Over the past decade, the MOSFET has continually been scaled down in size such as the typical channel length was once several microns [Yusnira Husani *et al,* 2010]. At present time the modern integrated circuits are research on incorporating MOSFET with channel lengths of ten nanometres [San Jose *et al*, 2001]. Producing MOSFET with channel length much smaller than a micrometer is a challenge and the difficulties of semiconductor device fabrication are always a limiting factor in advancing IC (integrated circuit) technology. The small size has created electrical operational problem in the MOSFET such as threshold voltage, sub threshold voltage and leakage current. SOI n-MOSFET technology has become another advanced technology for very large scale integrated (VLSI). The advantage of SOI is the capability to provide deep submicron VLSI device for generating high speed, low power and low voltage supply. SOI technology also preferred for its advantages such as full dielectric isolation and reduction of junction capacitance and kink effect.and allows them to be spaces closely. Hence, the bandwidth efficiency is significantly increased due to orthogonal subcarriers and then more sub channels can be placed into the same bandwidth.

In recent year, silicon on Insulator (SOI) has attracted considerable attraction as a potential alternative substrate for low power applications [Srinivasa R. Banna *et al,* 1995]. We have two types of SOI, which are fully depleted (FD) and partially depleted (PD) depending on the extent of the silicon thickness on the insulator. Usually, the thickness of silicon for PD SOI device is in range between 100nm to 500 nm. The major difference between FD and PD is the insertion of an insulation layer beneath the device. In this paper, three electrical characteristics are simulated which are threshold voltage, sub threshold voltage and leakage current with Constant channel length, 0.4 µm. This paper presents electrical characteristics comparison between partially-depleted SOI and n-MOS devices. The study involves the development of SOI device by Silvaco software. Results obtained from the study revealed that the electrical characteristics such as threshold voltage, leakage current and subthreshold swing of partially-depleted SOI devices are outperformed than that of bulk-Si devices.

2. SOI Fundamentals

Silicon-On-Insulator (SOI) is a new way of starting the chip making process, by replacing the bulk silicon wafers (approximately 0.75 mm thick) with wafers which have three layers; a thin surface layer of silicon (from a few hundred Angstrom to several microns thick) where the transistors are formed, an underlying layer of insulating material and a support or "handle" silicon wafer. The insulating layer usually made of silicon dioxide and referred to as the "buried oxide" or "BOX", is usually a few thousand Angstroms thick. When transistors are built within the thin top silicon layer, they switch signals faster, run a lower voltages and much less vulnerable to signal noise from background cosmic ray particles. Since on an SOI wafer each transistor is isolated from its neighbour by a complete layer of silicon dioxide, they an immune to

*Corresponding author **Gautam Kumar Jaiswal** is M.Tech Scholar; **Anil Kumar, Rajeev Paulus** and **Mayur Kumar** are working as Asst Prof; **A.K.Jaiswal** as HOD

"latch-up" problems and can spaced closer together than transistors built on bulk silicon wafers. Building circuits on SOI allows for more compact chip designs, resulting in smaller IC devices (with higher production yield) and more chips per wafer (increasing fab productivity). In Silicon on Insulator (SOI) Fabrication technology Transistors are built on a silicon layer resting on an Insulating Layer of Silicon dioxide (SiO2). The insulating layer is created by flowing oxygen onto a plain silicon wafer and then heating the wafer to oxidize the silicon, thereby creating a uniform buried layer of silicon dioxide. Transistors are encapsulated in SiO2 on all sides. The blow figure shows a typical NMOS Transistor with Bulk CMOS Process and with SOI Process.

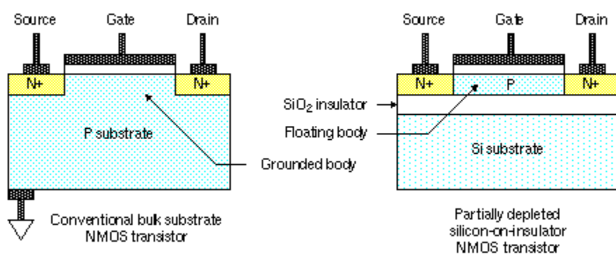


Fig.2 Bulk NMOS Transistor vs SOI NMOS Transistor

CMOS integrated circuits are almost exclusively fabricated on bulk silicon substrates for two well-known reasons: the availability of electronic grade material and because a good quality oxide can be readily grown on silicon, a process which is not possible on germanium or on compound semiconductors. Yet modern MOSFET's made in silicon are far from the ideal structure [Won-Ju Cho *et al*, 2004]. Bulk MOSFET's are made in silicon wafers having a thickness of approximately 800 micrometers but only the first micrometre at the top of the wafer are used for transistor fabrication. Interactions between the devices and the substrate give rise to a range of unwanted parasitic effects.

3. Simulation tools and Methodology Description

3.1 Athena Inputs and Outputs

Athena framework integrates several process simulation modules within a user-friendly environment provided by Silvaco TCAD interactive tools.

Fig.1 Athena Input and Output Block diagram

Athena has evolved from a world-renowned Stanford University simulator SUPREM-IV, with many new capabilities developed in collaboration with dozens of academic and industrial partners. Athena provides a convenient platform for simulating processes used in semiconductor industry: ion implantation, diffusion, oxidation, physical etching and deposition, lithography, stress formation and silicidation.

3.2 Atlas Inputs and Outputs

ATLAS produces three types of output. The run-time output provides a guide to the progress of simulations running, and is where error messages and warning messages appear. Log files store all terminal voltages and currents from the device analysis, and solution files store two- and three dimensional data relating to the values of solution variables within the device for a single bias point.

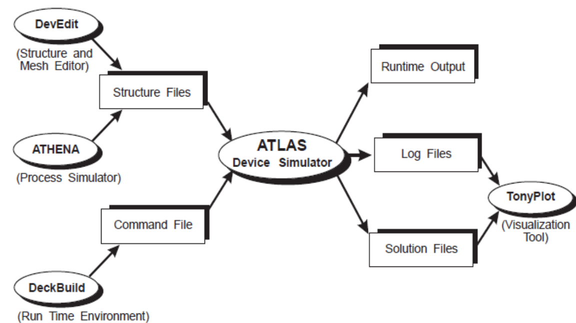


Fig.3 Atlas Input and Output Block diagram

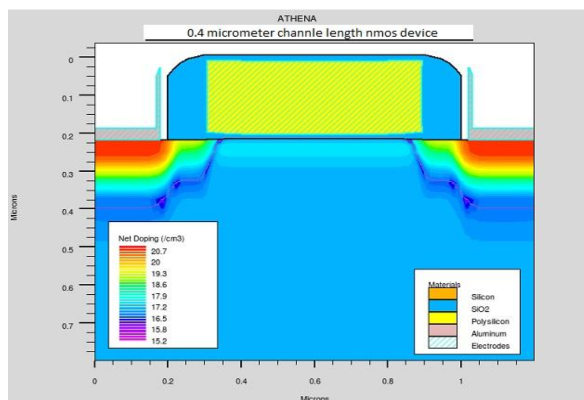
4. Result and Discussion

There are major part of this research is we have compare bulk nmos devices with the partially depleted soi devices. The measuring parameters Threshold voltage, sub threshold voltage and leakage current in the partially depleted soi here also described the kink effect in the partially depleted silicon on insulator devices.

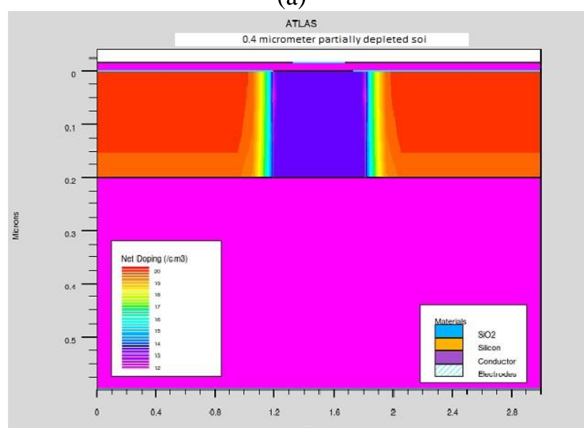
4.1 Threshold voltage and leakage current in 0.4 micron bulk nmos and partially depleted SOI

Process variability alters the ratio of forward and reverse diode leakages, which will establish new balanced voltages. Shorter channels will also produce more impact ionization, resulting in more history effect. Conducting Hot Electron generation also simultaneously presents as degradation in device current. This degradation's dependence on channel length, and hence the electron-hole pair generation for a typical production CMOS technology. Shorter channels also produce bodies with less total volume. Smaller bodies contain less charge, and the decreased volume reduces the time necessary to achieve large excursions in body potential. Voltage of the supply affects junction leakage, and will affect the body potential. Of importance is not only the magnitude of forward and reverse leakage currents, but changes in the ratio of forward bias current to reverse bias current. Temperature strongly affects junction leakage and device threshold voltage, as well. Lower threshold voltage at higher temperatures increases the portion of the electron energy distribution capable of ionizing silicon lattice points.

Temperature also affects the leakages of the junctions themselves, directly affecting body charge content. The most prominent electrical property of the PD-SOI device is the History Effect. I-V characteristics of the MOSFET built in PD-SOI are no longer constant, but dependent on the amount of charge contained in the body of the device at any given time. The charge content of the body and the distribution of that charge caused by gate, source, and drain potentials determine the behavior of the device. Charge in the body is directly related to the potential of the body.

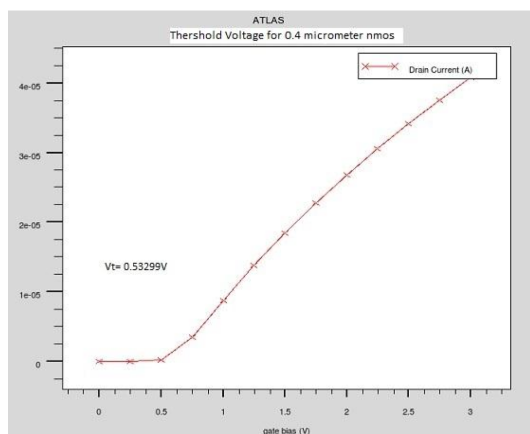


(a)

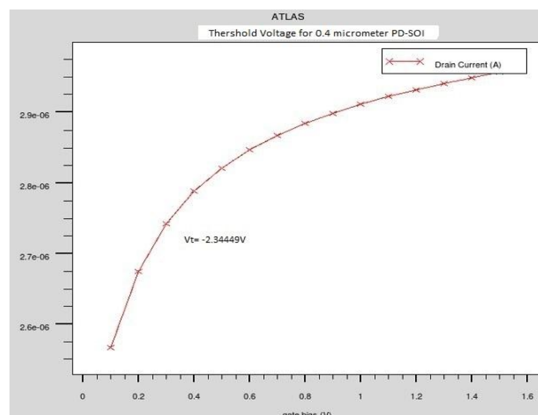


(b)

Fig.4 Structure of 0.4 µm bulk nmos (b) Structure of 0.4 µm PD-SOI



(a)



(b)

Fig.5 (a) Thershold Voltage Plot of 0.4 µm bulk nmos (b) Thershold Voltage Plot of 0.4 µm PD-SOI

ATLAS output for threshold voltage of nmos and patially depleted soi is extracted as below:

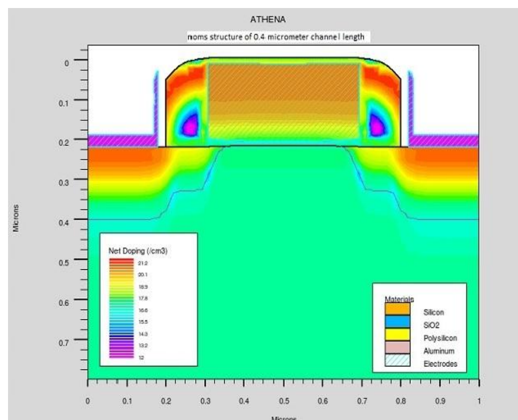
```
EXTRACT> extract name="nvt"
(xintercept(maxslope(curve(abs(v."gate"
),abs(i."drain"))))  -
abs(ave(v."drain"))/2.0)
nvt=0.53299V(Thershold Voltage of nmos)

EXTRACT> extract name="vt"
(xintercept(maxslope(curve(v."gate",abs
(i."drain"))))
abs(ave(v."drain"))/2.0)
vt=-2.34449 V (Thereshold voltage for
Partially depleted SOI)
```

This again affects the potential where the current into the body is balanced with the current out of the body. Temperature also affects the leakages of the junctions themselves, directly affecting body charge content. The dependence of MOSFET threshold voltage on substrate bias is well known. Conceptually, body bias's effect on threshold voltage may be explained by how strongly this potential reverse-bias the junctions, which must be overcome by gate drive. The magnitude of charge contained in the body is dependent on a number of factors which include: Previous state of transistor, Schematic position of transistor (possible source, drain voltage ranges), Slew rate of input, and load capacitance, Channel length and processing corner, Operating supply voltage, Junction temperature, Operating frequency and specific switching factor.

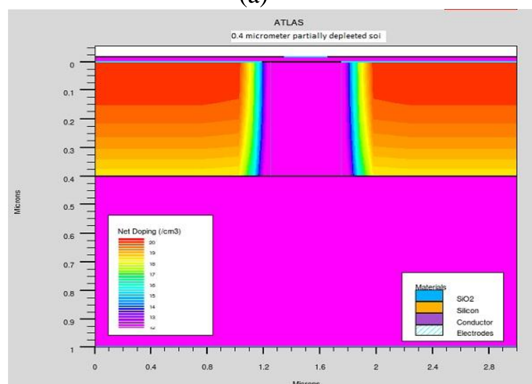
ATLAS output for leakage current of nmos and patially depleted is extracted as below:

```
gateox=155.512 angstroms (0.0155512 um)
X.val=0.49
nxj=0.176427 um from top of first
Silicon layer  X.val=0.1
n1dvt=0.608208 V X.val=0.49
n++ sheet rho=31.025 ohm/square
X.val=0.05
ldd sheet rho=5094.45 ohm/square
X.val=0.3
```

```
chan surf conc=4.02714e+16 atoms/cm3
X.val=0.45
nsubvt=0.0888883
Leak=1.3134e-05 A/um (Leakage Current
in nmos)
ATLAS>
EXTRACT> init inf="pdsoi.log"
EXTRACT> extract name="ids_leakage" max
(abs (i."drain"))
ids_leakage=5.09605e-05 A/um (Leakage
current in partially depleted SOI)
```

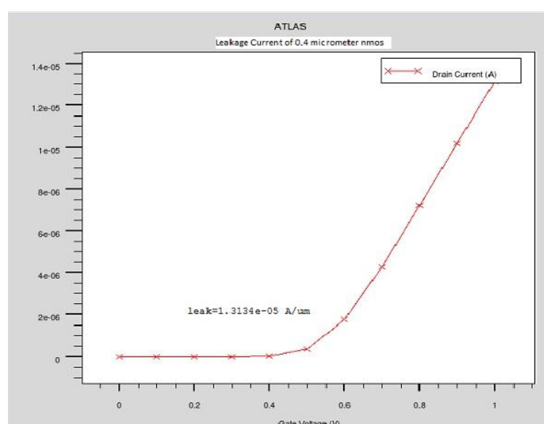


(a)

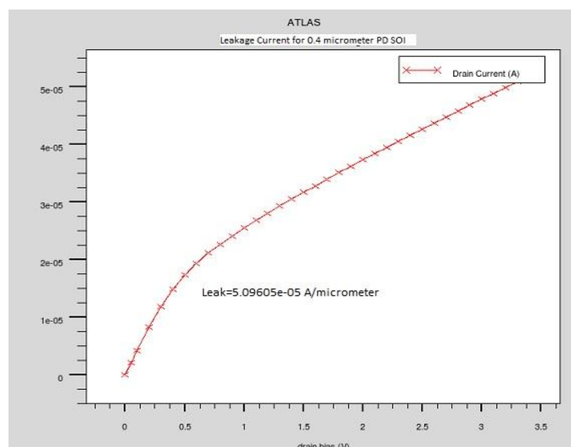


(b)

Fig.6 (a) Structure of 0.4 µm bulk nmos (b) Structure of 0.4 µm PD-SOI



(a)



(b)

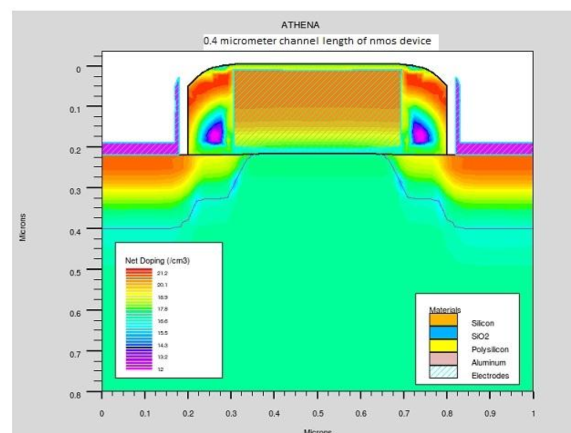
Fig.7 (a) Leakage current of 0.4 µm bulk nmos (b) Leakage Current of 0.4 µm PD-SOI

ATLAS output for leakage current of nmos and patially depleted is extracted as below:

gateox=155.512 angstroms (0.0155512 um) X.val=0.49
nxj=0.176427 um from top of first Silicon layer X.val=0.1
n1dvt=0.608208 V X.val=0.49
n++ sheet rho=31.025 ohm/square X.val=0.05
ldd sheet rho=5094.45 ohm/square X.val=0.3
chan surf conc=4.02714e+16 atoms/cm3 X.val=0.45
nsubvt=0.0888883
leak=1.3134e-05 A/um (Leakage Current in nmos)
ATLAS>
EXTRACT> init inf="pdsoi.log"
EXTRACT> extract name="ids_leakage" max(abs(i."drain"))
ids_leakage=5.09605e-05 A/um (Leakage current in partially depleted SOI)

4.2. Subthreshold Analysis

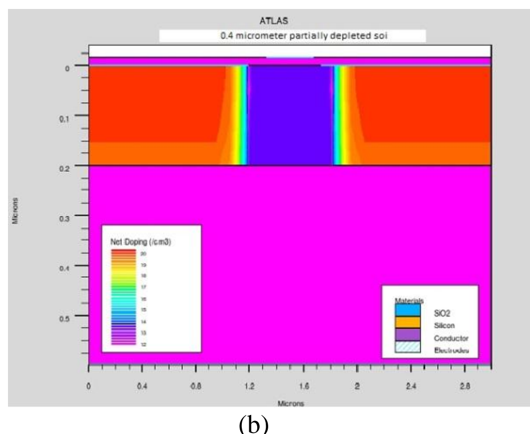
The subthreshold slope is defined as the inverse of the slope of the Id (Vg) curve in the subthreshold regime, presented on a semi logarithmic plot.



(a)

On a log plot the subthreshold current appears as a straight line. The inverse of the slope of that line is called inverse sub threshold slope or simply sub threshold slope. It is expressed in volts per decade.The lower the value of sub

threshold slope, S, the more efficient and rapid the switching of the device from the off state to on state.



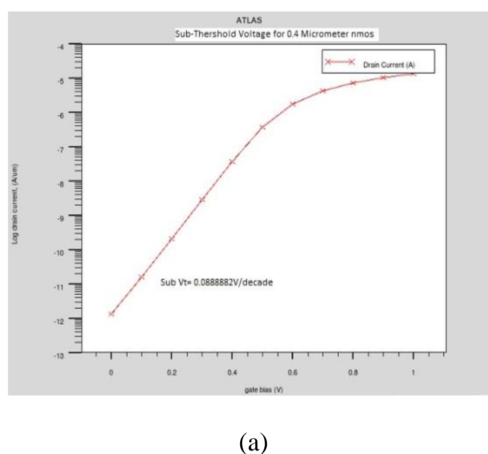
(b)

Fig.8 (a) Structure of 0.4 µm bulk nmos (b) Structure of 0.4 µm PD-SOI

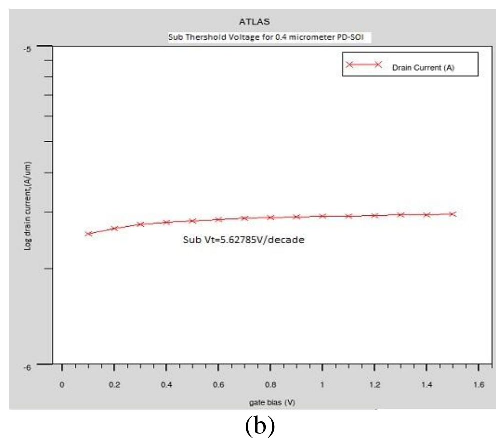
The Subthreshold behavior of an SOI MOS device depends on the thickness of the silicon thin-film, the doping density of the silicon thin-film, and the channel length. When the silicon thin-film is thick, partially depleted, the sub threshold slope of the SOI n-MOSFET device is similar to that of the bulk devices. For a partially depleted device, a higher silicon thin film doping density leads to worse inverse sub threshold slope silica to the bulk device.

ATLAS Output for subthershold voltage of nmos and partially depleted soi

```
ATLAS>
EXTRACT> init inf="nmos_1.log"
EXTRACT> extract name="nsubvt"
1.0/slope(maxslope(curve(abs(v."gate"),
log10(abs(i."drain")))))
nsubvt=0.0888882 V/decade

ATLAS>
EXTRACT> init inf="pdsoi_1.log"
EXTRACT> extract name="subvt"
1.0/slope(maxslope(curve(v."gate",log10
(abs(i."drain")))))
subvt=5.62785 V/decade
```



(a)



(b)

Fig.9 (a) Subthershold slope of 0.4 µm bulk nmos (b) Subthershold slope of 0.4 µm PD-SOI

The most prominent electrical property of the PD-SOI device is the History Effect. I-V characteristics of the MOSFET built in PD-SOI are no longer constant, but dependent on the amount of charge contained in the body of the device at any given time. The charge content of the body and the distribution of that charge caused by gate, source, and drain potentials determine the behavior of the device. Charge in the body is directly related to the potential of the body. The dependence of MOSFET threshold voltage on substrate bias is well known. Conceptually, body bias's effect on threshold voltage may be explained by how strongly this potential reverse-bias the junctions, which must be overcome by gate, drive.

Table 1 Comparison Result From Tony Plots For 0.4µm NMOS & PD-SOI

Parameters	Bulk n-type mos	Partially depleted soi
Vth (V)	0.53299V	-2.34449 V
Sub Vth (V/decade)	0.0888882 V/decade	5.62785 V/decade
Ids_leakage(A/µm)	1.3134e-05 A/µm	5.09605e-05 A/µm

5. Conclusion

This paper has presented the electrical characteristics and performance comparison between partially-depleted SOI and n-MOS devices using Silvaco T-CAD Simulator. The comparison of the both technology shows the various electrical characteristics of n-MOSFET through implementing partially-depleted technology as compared to the bulk n- MOSFET device structure. Based on the simulation results we obtained, it can be concluded that as compared to bulk-Si devices, partially-depleted SOI devices shows the ability to improve the electrical characteristics specifically lower threshold voltage, steeper subthreshold swing and lower leakage current. Even though SOI gives ability to minimize the parasitic effect will also appear increasing of subthreshold and leakage current when the scale was reduced in SOI continuously.

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Authors

Gautam Kumar Jaiswal is student of M.Tech. ECE (MCE) in the Department of Electronics & Communication Engineering in SHIATS-DU, Allahabad.He received his B.Tech degree from Sachdeva Institute of Technology, Mathura, (U.P.) Affiliated to Gautam Buddh Technical University, Lucknow (U.P.).He is Graduate Student Member of IEEE Member No. 92934610 in Uttar Pradesh section.

Anil Kumar is Assistant Professor in ECE Department at SHIATS-DU Allahabad. He obtained B.E from MMMEC Gorakhpur in ECE, M.Tech. from IIT BHU Formerly IT B.H.U. Varanasi in Microelectronics Engg. And he has done Ph.D. from SHIATS-DU Allahabad. He guided various projects & research at undergraduate & postgraduate level. He published many research papers in different journals. He has more than 10 years teaching experience and actively involved in research and publications. His area of interest includes Antenna, microwave, artificial neural network and VLSI.

A.K. Jaiswal is Prof. and Head of ECE-Department at SHIATS-Allahabad. He obtained M.Sc. in Tech. Electronics & Radio Engg. from Allahabad University in 1967. He guided various projects & research at undergraduate & postgraduate level. He has more than 40 years Industrial, research and Teaching experience and actively involved in research and publications. His area of interest includes Optical Networks and satellite communication.

Dr. Rajeev Paulus Working as an Assistant Professor in the Department of Electronics and Communication Engineering in SHIATS, Allahabad. He received the degree of M.Tech from MNNIT, Allahabad. He received the degree of Ph.D. from SHIATS, ALLAHABAD. He has presented and published various research papers in national and international Journals and conferences. He is currently focusing on the area of wireless sensor and adhoc network, high speed data network.

Mayur Kumar is Asst. Prof. at SHIATS-DU Allahabad. He obtained B.E from North Maharastra University in Electronics Engineering, M.Tech. from SHIATS-DU Allahabad in communication System Engineering. He has more than 10 years teaching. Experience and actively involved in research and publications.