

Research Article

Performance Analysis of Convolutional Encoder for Rate Change

Sneha W. Bawane^{Å*} and V.V.Gohokar^Å

^ÅDept of Electronics and Telecommunication, SSGMCE Shegaon, Amravati University, Maharashtra-444203, India

Accepted 10 April 2014, Available online 15 April 2014, Vol.4, No.2 (April 2014)

Abstract

In this paper, a modified FPGA scheme for the convolutional encoder is presented in OFDM baseband processing systems. The proposed designs shows convolutional encoder with constraint length 9. Convolutional encoding is a Forward Error Correction (FEC) technique used in continuous one-way and real time communication links. This paper presents the performance of convolutional encoder by changing the data rates of convolutional encoder on Xilinx.

Keywords: Convolutional encoder, Data Rates, FPGA, VHDL, Xilinx 8.1i

1. Introduction

The convolutional encoder maps a continuous information bit stream into a continuous bit stream of encoder output. Convolutional encoding is a method of adding redundancy to a data stream in a controlled manner So that it gives the destination the ability to correct bit errors without asking the source to retransmit. Convolutional codes, and other codes which can correct bit errors at the receiver, are called forward error correcting (FEC). The convolutional encoder is a finite state machine, which is a machine having memory of past inputs and also having a finite number of different states.

Convolution codes are better codes for error controlling performance. Convolutional encoder outputs are not only associated with the encode elements at present, but also affected by several ones before. These are one of the powerful and widely used class of codes. The convolutional codes are having many applications, that are used in voice band modems, wireless standards (such as 802.11), deep-space communications and in satellite communications. These codes play a role in low-latency applications such as speech transmission. (Yan Sun¹, Zhizhong Ding², 2012), (A. Msir, F. Monteiro, 2004), (Zafar Iqbal, Saeid Nooshabadi, Heung-No Lee, 2012) Convolutional codes are mainly specified by three parameters; (n, k, m) .

n = number of output bits

k = number of input bits

m = number of memory registers

Where, $n > k$

The quantity k/n is called as code rate and it is a measure of the efficiency of the code. Commonly k and n parameters ranging from 1 to 8, m from 2 to 10 and the code rate from 1/8 to 7/8 except for deep space

applications where code rates as low as 1/100 or even longer have been employed. The quantity L is called the constraint length of the code and is defined by

$$\text{Constraint Length, } L = k(m-1)$$

The constraint length L represents the number of bits in the encoder memory that affect the generation of the n output bits. The constraint length L is also referred to by the capital letter K , which is confusing with the lower case k , which represents the number of input bits. In some books K is defined as equal to product of k and m . Often in commercial specifications, the codes are specified by (r, K) , where r = the code rate k/n and K is the constraint length.

2. Method

In Convolutional Encoder shifting is done by using shift registers. Delays can also be used in place of shift registers. Result out as coded bit stream.

2.1 Rate 1/3

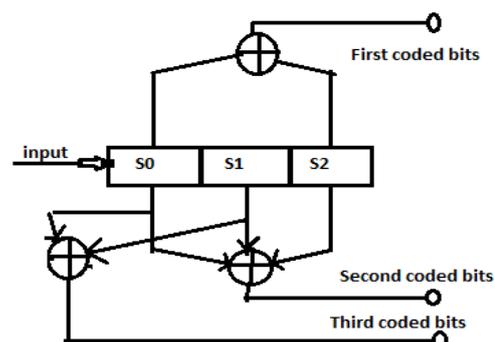


Fig.1 Convolutional Encoder for rate 1/3

*Corresponding author **Sneha W. Bawane** is a ME student and **Dr V.V.Gohokar** is working as Professor

If initially Input=0 and S0=0, S1=0, S2=0
 So, Output=000
 Input=1, 1 is shifted to S0
 S0=1, S1=0, S2=0
 Thus, Output=111 and so on

2.2 Rate 1/2

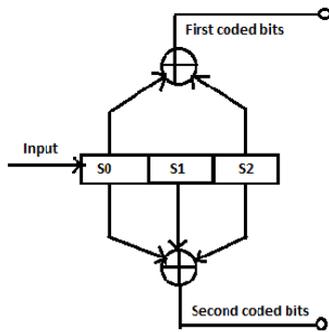


Fig.1 Convolutional Encoder for rate 1/2

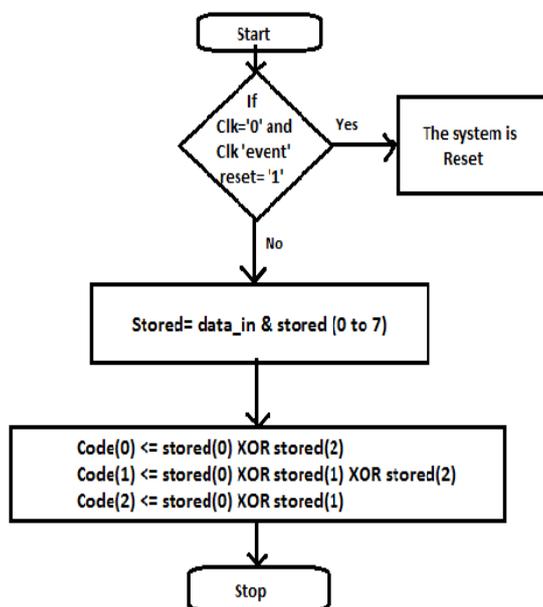
If initially Input=0 and S0=0, S1=0, S2=0
 So, Output=000
 Input=1, 1 is shifted to S0
 S0=1, S1=0, S2=0
 Thus, Output=11 and so on

2.3 Rate 2/3

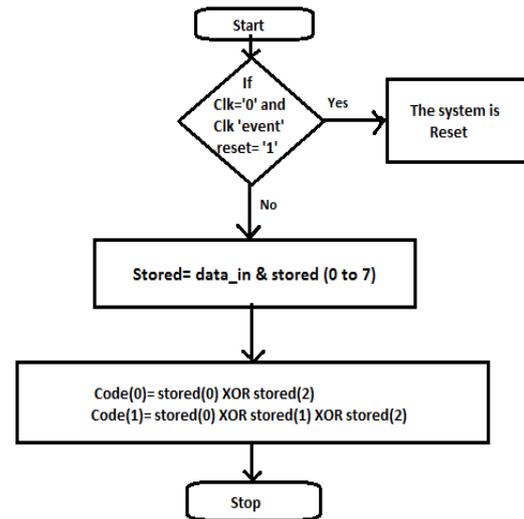
From Fig.1, If Input=00
 S0=0, S1=0, S2=0
 Output=000
 Input=11
 Then, S0=1, S1=1, S2=0
 Output=101 and so on

3. Workflow

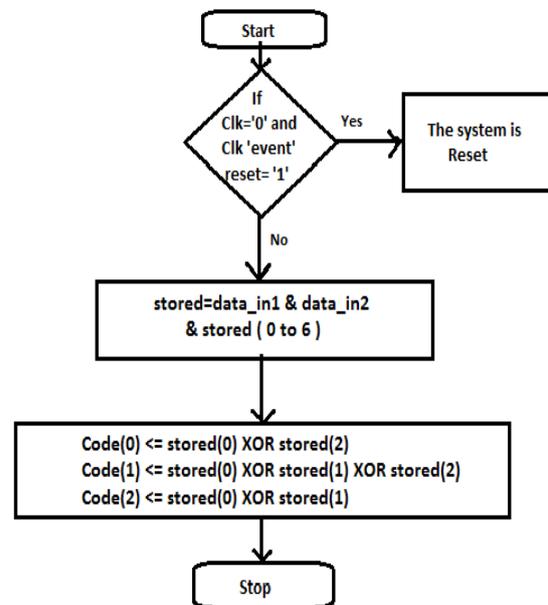
3.1 Rate 1/3 convolutional Encoder



3.2 Rate 1/2 convolutional Encoder

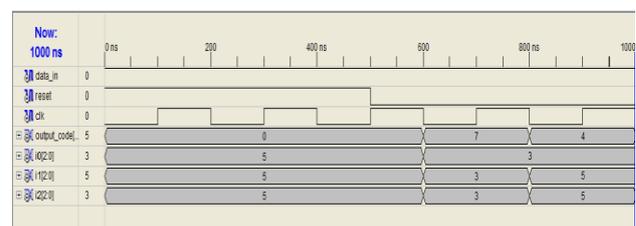


3.3 Rate 2/3 convolutional Encoder

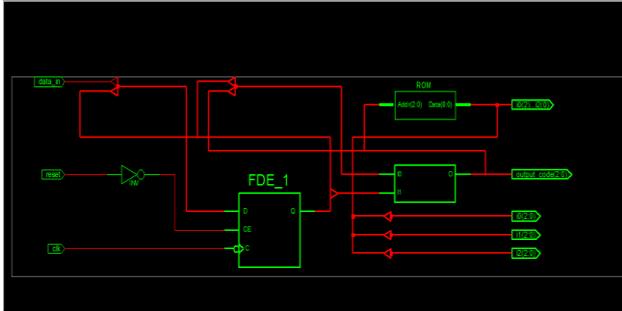


Above workflow describes the design of convolutional encoder. It shows conditions to perform designing.
 clk = not(clk) after 100 ns;
 reset = '1','0' after 500 ns;
 data_in is '1' for 1000ns then '0' upto 1500ns and it again becomes '1' after 1500 ns until 2000 ns;

4. Results and RTL Schematics



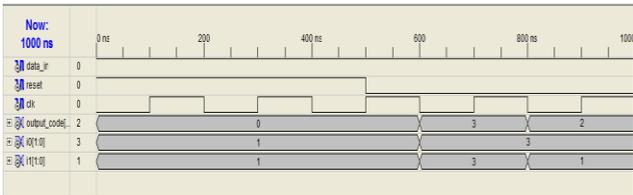
(i)



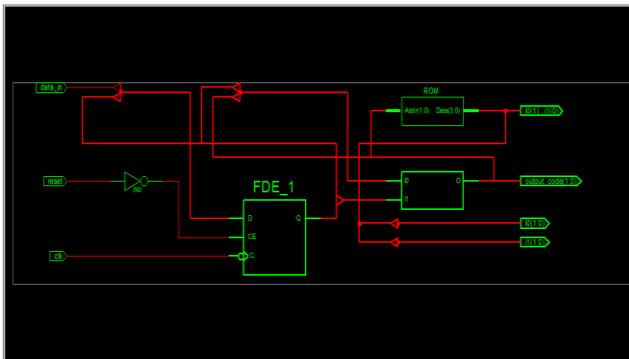
(ii)

Fig.2(a) For data rate 1/3, (i) Result (ii) RTL Schematic

Fig.2(a)-(i) shows test bench waveform for rate 1/3 convolutional encoder. The output is converted into soft decision, such that-
 0 → -3(101)
 1 → +(011)



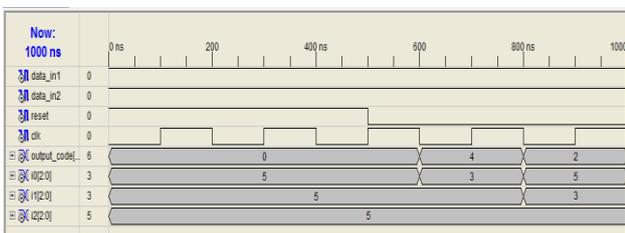
(i)



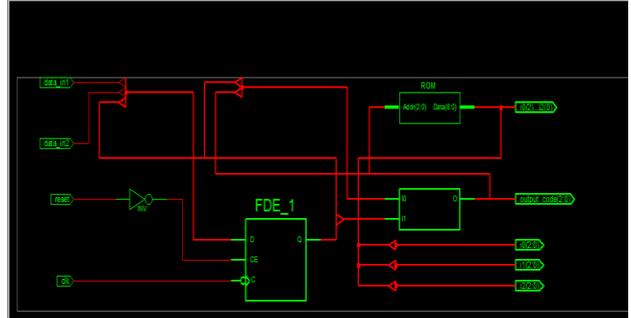
(ii)

Fig.2(b) For data rate 1/2, (i)Result (ii)RTL Schematic

Fig.2(b)-(i) shows test bench waveform for rate 1/2 convolutional encoder. The output is converted into soft decision, such that-
 0 → -3(11)
 1 → +3(11)



(i)



(ii)

Fig.2(c) For data rate 2/3, (i)Result (ii)RTL Schematic

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	4	1200	0%
Number of Slice Flip Flops	3	2400	0%
Number of 4 input LUTs	7	2400	0%
Number of bonded IOBs	16	144	11%
Number of GCLKs	1	4	25%

Fig.2(d) Design summary



Fig.2(e) FPGA implementation

Conclusions

Convolutional encoder used in digital communication and WLAN. Performance has done by changing the data rates of convolutional encoder as 1/2,1/3 and 2/3.Results out by convolutional encoding. It concludes that the convolutional encoding is better and easy technique for communication.

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