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Research Article

High Performance Adaptive Sigma Delta Modulator Design (using LMS Algorithm) for Performance Enhancement of DSP Processors and FPGA Synthesis of the Proposed Architecture

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Abstract

Enhancement of the performance and speed of the Digital Signal processing processors are the major challenge due to its wide spread real world applications. At the same time high quality (less erroneous) and high speed digital inputs are required for these DSP Processors. Hence the high performance and high speed A/D or D/A converter design is the another major issue for performance and speed matching with these DSP processors. In this paper a novel technique is introduced to enhancement the performance of the Sigma Delta modulator using Least Mean Square (LMS) algorithm. This LMS algorithm is used to minimize the quantization error and hence the performance enhancement. The circuit implementation requires limited additional circuits for the proposed technique. For design and implementation of the proposed sigma delta modulator a Simulink model is constructed for the oversampled Sigma Delta Modulator with applied LMS algorithm. This model is verified by two types of simulations like Matlab and ModelSim. The proposed architecture is also synthesized for FPGA implementation.

Keywords: *Analog to Digital Converter (ADC), Configurable Logic Block (CLB), Digital Signal Processing (DSP), Field Programmable Gate Array (FPGA), Harvard architecture, Least Means Square (LMS), Look up Table (LUT), Power Spectral Density (PSD).*

1. Introduction

DSP processors have wide spread applications in daily life products (embedded systems), industry, military, various fields of communications and different organizations and universities research units etc. so modern research is concerned with the Performance Enhancement and speed of the DSP processors **(Sinha P. *et al* 2005; Barkley Design Technology Inc. 2004)**. Moreover DSP processors are more advantageous than old analog signal processing processors where they use fixed hardware components for signal processing and these hardware components are highly dependent on ambient parameters like temperature, pressure, humidity etc. These can change the electrical property of the hardware components and hence affects the signal processing and performance of the DSP processors. Since the DSP processors process the signal only with their digital values hence these high speed processors need high speed digital input data for processing. Thus high speed A/D or D/A converter is required for speed matching of the high speed DSP processors. There are various techniques were developed. Sigma Delta Modulator is an ideal candidate for that. They are now widely used in many applications in digital signal processing fields. Due to development of VLSI technology it is required high conversion speed, low cost, low bandwidth, low power and high resolution ADCs. Sigma Delta Modulation **(Park S.; Kaur S. *et al* 2013; Couch II L. W. 2005; Béchir D. M. *et al* 2007)** is basically an oversampling analog to digital converter. This type of converter is based on the principle that the sampling rate is much higher than the Nyquist rate. For high resolution purpose these oversampled noise shaping converters take more advantage. Thus the noise reduction in the converters is the key factor to enhance the performance of the converters. This also provides the high quality data for further processing.

The main objective of this paper is to reduce quantization noise generated due to sigma delta modulation and hence improve the performance. This is done by applying adaptive algorithm like Least Mean Square (LMS) algorithm **(Proakis J.G. *et al* 2007**) on the Sigma-Delta modulator. The LMS adaptive FIR filters are the main component of many signal processing and communication systems and generally this type of adaptive filters are implemented in DSP Processors. These adaptive filters are used in feedback path of the sigma-Delta converter and they reduce the quantization

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noise very fast and hence improve the performance and speed of the converter. Due to feedback connection high stability and performance of the design can be achieved. This high performance and high speed proposed Sigma Delta modulator is essentially required for the high speed and high performance modern DSP processors. The speed and performance of DSP processors is enhanced by optimization of the instruction sets and efficient architecture design.

On the other hand FPGAs (Field Programming Gate Array) (**Dick C.H. *et al* 2001; DeGroat J. *et al* 2008; Hatai I. *et al* 2011; Saha A. *et al* 2009)** has emerged as highly programmable and hardware configurable devices. They can execute highly parallel signal processing functions which are described by Hardware Description Language (HDL). Due to their hardware flexibility any design can be executed and real time tested by FPGA. Any design can be represented by HDL (Verilog, VHDL) code and this code is converted into bit streams by the software tool-Xilinx ISE. This beat streams are downloaded on FPGA and then the FPGA is configured to the particular design. The FPGAs (**Xilinx, 2004; Wolf W. 2005)** consist of large number CLBs (Configurable Logic Block), IO blocks and router switches for interconnection among the CLBs. The bit streams of the corresponding design are downloaded on FPGA deice via JTAG cable which is connected between the PC and FPGA. The bit streams enter into FPGA through IO blocks of FPGA. These bit streams configure the router switches to connect the CLBs to construct the desired system. The CLBs are LUT (Look Up Table) based. Hence the FPGA can be utilized for implementation of the proposed design.

In this paper the proposed design is constructed by Simulink model and simulated by Matlab and ModelSim and synthesized for FPGA implementation.

2. General Overview of the Sigma Delta Modulator Architecture

2.1 Overview of the Sigma delta model

The performance enhancement of the Sigma Delta modulator is done by reducing the quantization noise. For this purpose LMS algorithm is applied on the sigma delta modulator architecture. In this section basic Sigma-Delta modulator's architectures **(Proakis J.G. *et al* 2007; Nandi S. *et al*)** are presented. The sigma-delta modulator is based on oversampling so by sampling at a frequency much greater than the signal bandwidth. Again a feedback loop is used to shape the quantization noise. Among the oversampling converters, Sigma Delta converters have achieved the most attraction due to its high-resolution applications and their noise shaping behavior. This is based on linear prediction of quantization noise and the circuit realization is very simple. Due to their oversampling nature, they act as the most suitable architectures for accurate low to moderately high frequency applications. A most general Sigma Delta modulator architecture can be described by an integrator, a comparator with feedback loop (1-bit DAC) and differentiator (sum/subtract between the input and feedback signal. The comparator is nothing but a 1-bit quantizer. The output of the quantizer depends on the sign of the integrator state. The comparator or quantizer output is sampled higher than Nyquist rate and sample value is hold until the next sampling instant. This design is modeled as equivalent discrete time model as the discrete or digital design is more practical design due to their technological advancements. This equivalent discrete sigma-delta modulator is nonlinear due to nonlinear characteristic of the quantizer. The Quantizer output is 1 when input is >=0 and -1 when input is <0. This discrete time model is first order model and the signal can be processed in digital domain. For more amount quantization noise reduction 2^{nd} or higher order designs developed. But they have complex circuitry and costly. However the sigma-delta modulator (analog-to-digital converters) can be used to supply the high quality inputs for high performance and speed matching of DSP processors. So it is essential to reduce the quantization noise developed on the sigma delta modulator very fast. The proposed design based on adaptive noise reduction which provides the performance enhancement of the sigma delta modulator and hence performance enhancement of the DSP processors.

2.1 Simulink Model of the Sigma delta model

High performance design of Sigma-Delta modulator is the main objective of this paper. So the second-order sigma-delta modulator is chosen because it has better performance than first order Sigma-Delta modulator. Thus a Simulink model of the second-order sigma-delta modulator is constructed and that Simulink model is shown in Fig.1. The integrators used in the second-order loop have individual delay. So the output y(n) will be y(n)=x(n)+y(n-1), where x(n) is input to the loop. The quantizer block is basically a stair step function. Neighboring points on the input axis are mapped to one point on the output axis. Output is symmetric about zero because the output is rounded to nearest method.

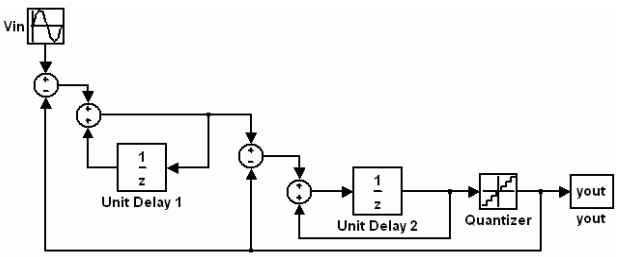

Fig.1 Simulink model of the Sigma-Delta modulator.

The quantization error occurs unless when the input signal is exactly equals one of its discrete values. The integrator accumulates the error over time. The feedback loop and quantizer minimize the error. Thus the quantizer output toggles about the input signal so that the average quantizer output is approximately equal to the average of the input. The proposed architecture is designed efficiently to eliminate the quantization noise generated by the quantizer.

3. A Novel Architecture of Sigma Delta Modulator Using LMS Algorithm

3.1 Basics of LMS Algorithms

Least Mean Square (LMS) algorithm is used in different adaptive filters to enhance the performance of that filters. In this section the basic concept of the LMS algorithm **(Proakis J.G. *et al* 2007; Heykin S. 2005)** is presented. The quantization noise is the noise which is developed by rounding the sample value of the input signal. The error i.e. quantization error e(n) defined as the difference between the desired response and the actual response. This error is minimized rapidly by changing the individual weights of the equalizer (filter coefficients) of the LMS algorithm connected in the feedback path of sigma-delta modulator.

The well-defined LMS algorithm **(Heykin S. 2005) is**: (Updated value of kth weight signal) = (Old value of kth weight signal) + (Step size Parameter) X (input signal applied to kth weight) (error signal) or **$w[n+1]=w[n]+\mu e[n]x[n]$** , where μ denote the step size which is proportional to quantization error and it is positive number. But it has upper limit or trade off. Greater than upper limit the system will be unstable and erroneous. In Least Mean Square (LMS) algorithm the error signal e(n) actuates the adjustments applied to the individual weight signals of the equalizer as the algorithm proceeds from one iteration to the next. The quantizer generates the quantization error which is not only inherent but also unavoidable. Thus LMS algorithm can be applied to the quantizer to minimize the error rapidly.

The important procedure is to realize the LMS algorithm by the weight signal w(n) which is the input signal of the multiplier whose another input is the original input x[n]. The output of the multiplier is connected to the quantizer. The quantizer is modeled as an adder which has two inputs, signal and quantization error. The difference between x(n) and y(n) (output of quantizer) is the quantization error. On the other hand the objective function is defined as the square of the error at time n and this is mathematically represented e2[n]=(x[n]-y[n])

Where the output of the quantizer can be expressed as y[n]=w[n]x[n]+N Then the expression for the weight signal is w[n]=∫e[n]dn. From this equation it is possible to structure adaptive ADC it is realized by a multiplier and integrator.

3.2 Proposed Architecture (Sigma delta modulator applying LMS Algorithm)

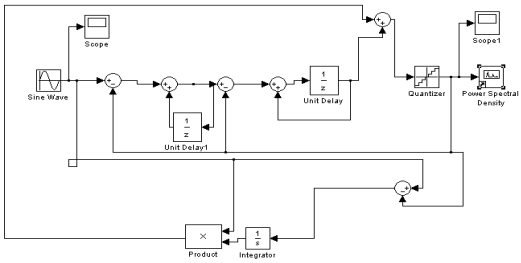

Fig.2 Proposed Simulink model of the Sigma-Delta modulator applying LMS algorithm

To reduce quantization noise generated by the sigma delta modulator depicted at fig.1, LMS algorithm is introduced into the diagram. To fulfill the purpose, a quantizer output along with the sine wave is fed into an integrator and then it is multiplied with the input. This produces a new architecture (proposed). The Simulink model of this proposed architecture is depicted on Fig.2.

4. Simulations of the Proposed Architecture using Matlab and ModelSim Simulators

The Sigma-Delta modulator is simulated by the two separate simulator tools like MATLAB and ModelSim. The model of sigma-Delta modulator applying LMS algorithm is also simulated by the above both simulators.

4.1MATLAB Simulation Results

The Simulink models of the both Sigma-Delta modulators (with or without LMS applied) are simulated by Matlab simulator and the simulation results of them are presented in this section.

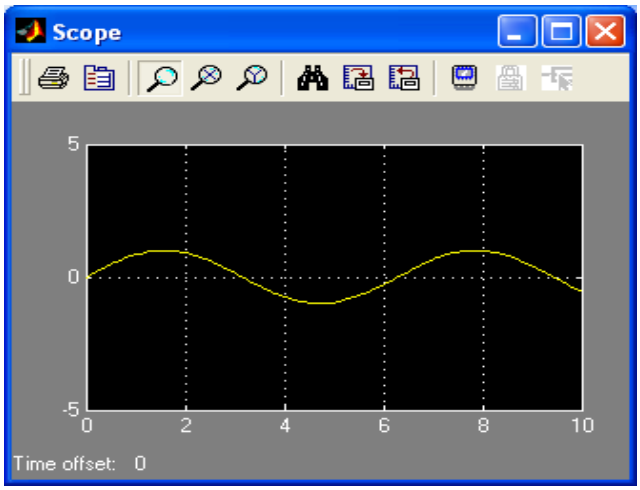

Fig.3a Scope output of a sine wave as input in Both cases

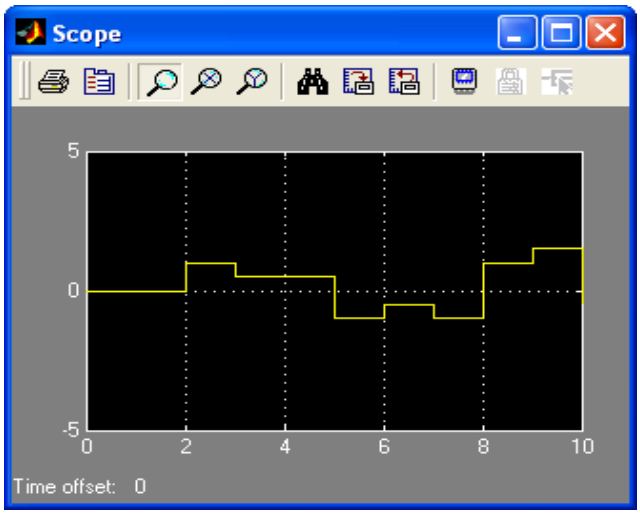

Fig.3b Scope output of the quantizer without applying the LMS Algorithm

The outputs at different points on the Simulink model are shown by Scope (a Simulink block for output signal). The Fig.3a to Fig. 3c depicts the outputs of the scopes after Matlab Simulation of the both Simulink models (Fig.1& Fig.2).

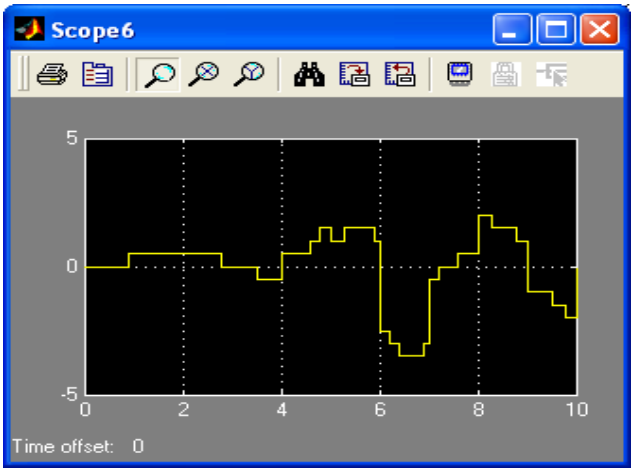

Fig.3c: Scope output of the quantizer after Applying LMS Algorithm

From Matlab simulation the power spectral density of the both models are derived. This is used for noise analysis and the performance analysis. The power spectral density of the both Sigma Delta modulators without or with LMS depicted in Fig. 4a & Fig. 4b respectively after Matlab Simulation. The output shows that the PSD is more than 1.5. Here the graphical outputs show that the peak value of PSD of the proposed Sigma Delta modulator is 0.8 where without applying LMS in Sigma Delta modulator has it peak value more than 1.5. Moreover 2nd peak is quickly downed in the proposed Sigma-Delta modulator. Thus in the proposed sigma-Delta modulator can reduce more noise than the existing one and have better performance.

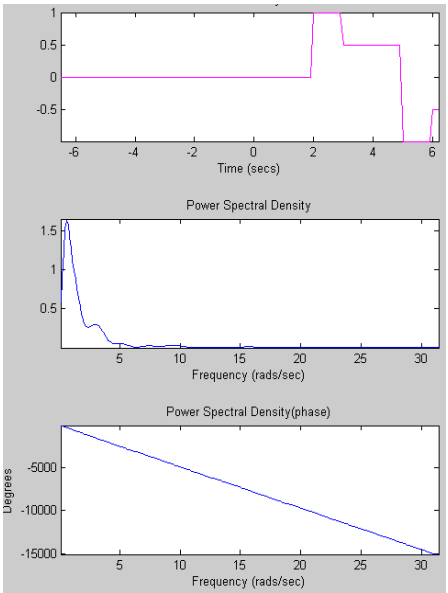

Fig.4a Power spectral density for existing sigma delta Modulator

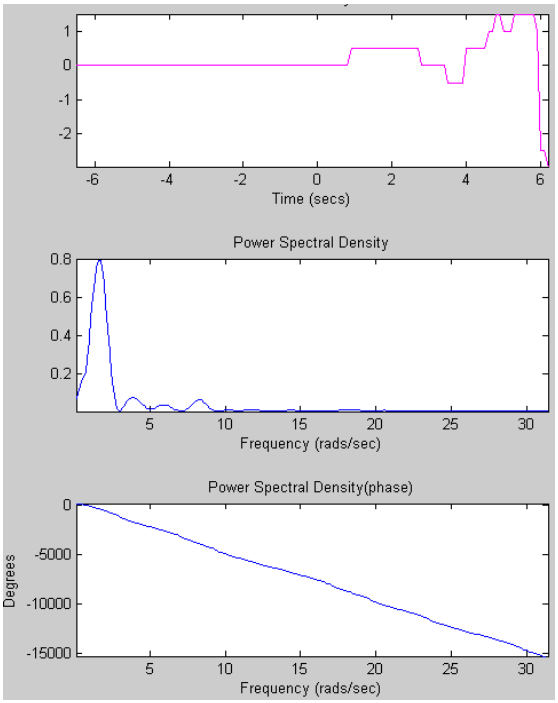

Fig.4b Power spectral density for the proposed architecture

4.2 ModelSim Simulation Results

The proposed Simulink models are simulated by Matlab simulator and they worked successfully. For these types of simulations i.e. ModelSim simulation HDL codes are required. Here the HDL codes are generated by MATLAB/SIMULINK/HDL-CODER. Some modifications are done in the proposed design (Fig.2) to generate the codes of the desired architecture. For HDL code (here Verilog) generation every block used in the Simulink model needs to be operated at the same sampling rate. Another problem is that the quantizer output is fed to sum 6 and later on to the integrator which contains digital value, but the integrator block is analog.

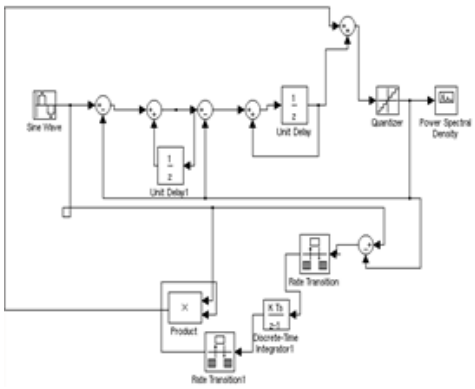

Fig.5 Revised model of Sigma-Delta modulator Applying LMS algorithm

To eliminate these problems in the proposed model some modifications are made to the existing Sigma Delta modulator which is depicted on the Fig.5. In the revised

model (Fig.5) Rate Transition blocks are used to match the Input and Output rates of the quantizer, sum6, integrator and the product block. The Integrator block is replaced by the Discrete Time Integrator block that can process the digital signal. The Verilog codes are generated as a file with extension .v .This code represents the proposed architecture.

This generated Verilog code is used for Modelsim simulation. With the Modelsim Simulator proposed Simulink model is tested and verified. For a specific input the result can be checked and the results of each of the blocks of the model are checked. Here the Mentor Graphics ModelSim SE 6.3f package is used for simulation.

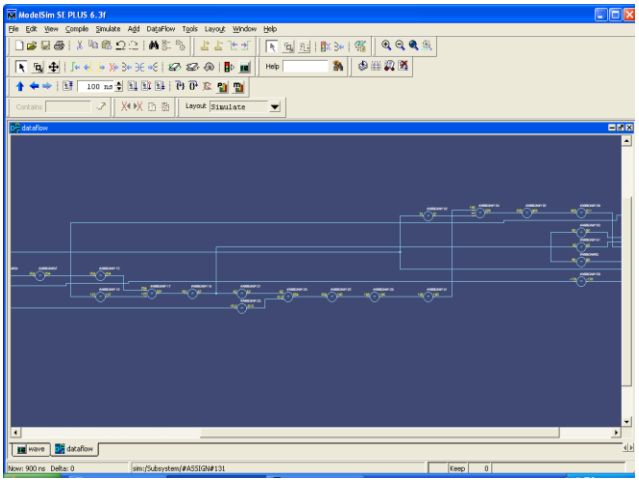

Fig.6a Dataflow Diagram for the whole module Without applying LMS Algorithm

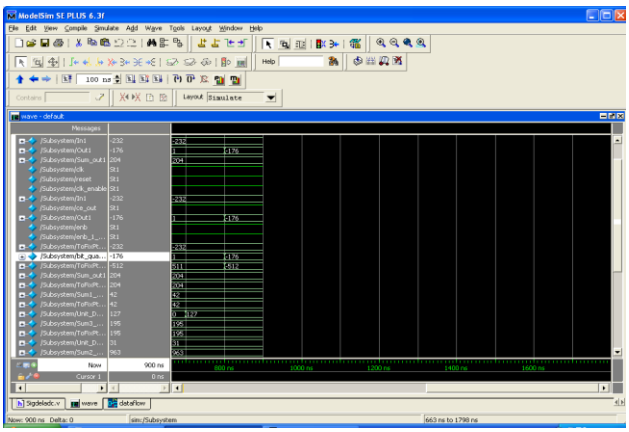

Fig.6b Waveform for the whole module without applying LMS Algorithm

For first compilation the Verilog file is converted the HDL code into ModelSim internal format. In Verilog, compiling is done on the module basis. After compiling the simulation is performed and the resulting waveform is examined. This corresponds to running the circuit in a virtual lab bench and checking the waveform in a virtual logic analyzer. The results of Simulation are obtained for the proposed model of Sigma Delta Modulator implementing LMS algorithm is given in this section. However, the results for the Sigma Delta Modulator without implementing LMS algorithm are also given for comparison between the two models.

Fig.6a to Fig.6d shows the Simulation results both in form of Dataflow Diagram and their GUI waveform for the both models.

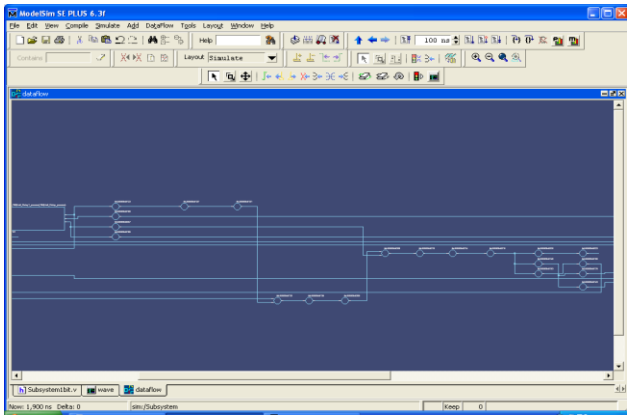

Fig.6c Dataflow Diagram for the whole module After applying LMS Algorithm

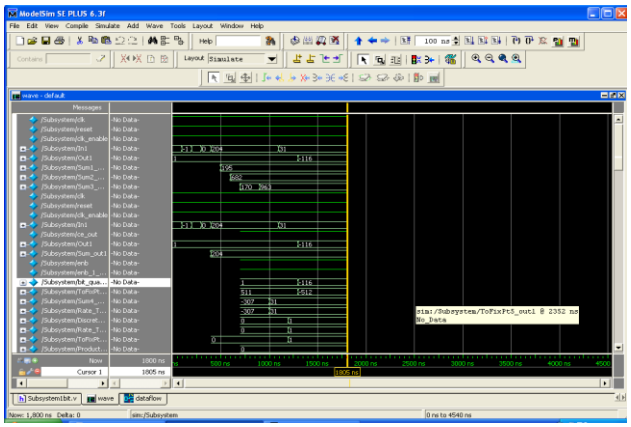

Fig.6d Waveform for the whole module after applying LMS Algorithm

But the code generated by HDLCODER suffers from one drawback that the code cannot be used for synthesis. The reason behind this is the Real data types are not synthesizable. The Real data type in the generated Verilog code as the model is used for converting the analog signal into digital. So, to eliminate this Real data types from the Verilog code, the Data Type Conversion blocks are used in the model. The purpose of the Data Type Conversion block is to convert the data according to the user choice. Here the double or Real data type is converted to the Fixed-point number using the Data Type Conversion block. Real data types are not synthesizable but the Fixed-point data types are Synthesizable. However only one problem remained regarding the quantizer block as it can only process double or single data types. For this reason the quantizer block is replaced by the 1-bit Quantizer or Sign block. The output for the Sign block is 1 for positive input, -1 for negative input, and 0 for 0 input. The new 1-bit quantizer block can be operated without the Real Data

type. Hence with this modification another Simulink model is developed which is shown in Fig. 7. The HDL-CODER can now generate the synthesizable code for the corresponding Simulink model. The revised model (Fig.7) is assigned into Subsystem module with all the blocks grouped into it for easy operation. Chirp Signal which is a time variable sinusoidal signal for generating non Real data types is fed into this Module.

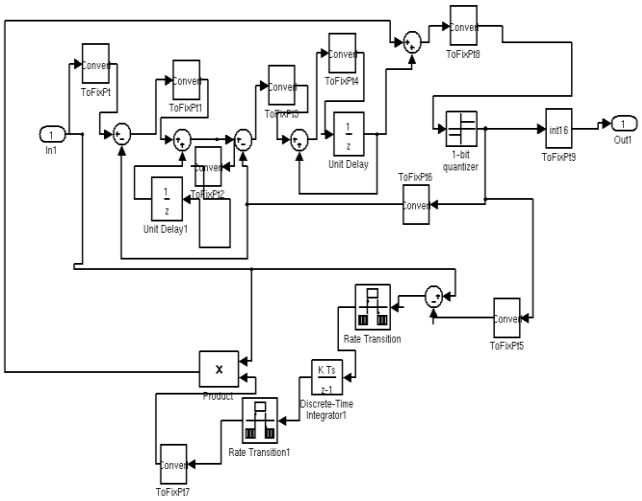

Fig.7 Revised Architecture of proposed Sigma Delta Modulator

5. Synthesis Results for FPGA based Implementation of the Proposed Sigma Delta Modulator Architecture

The proposed Sigma Delta modulator architecture and existing Sigma Delta modulator are synthesized for FPGA technology (FPGA Vertex-IV). Both designs are described by Verilog -a Hardware Description Language (HDL) (**Thomas D. E., *et al* 2002**). These Verilog codes are synthesized by Xilinx ISE software for FPGA synthesis and implementation. Xilinx ISE (integrated software environment) controls all aspects of the development flow.

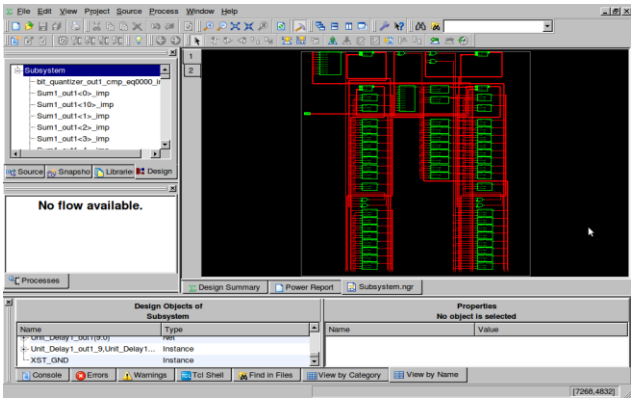

Fig.8a Snapshot of all the components of Sigma Delta Modulation without applying LMS algorithm

Project Navigator is a graphical interface for users to access software tools and relevant files associated with a project. In the Synthesis process after checking the syntax of the code, ISE generates Synthesis Reports, RTL Schematic diagram and Technology schematic of the proposed scheme and finally produced the bit stream for FPGA implementation. These synthesis results are very helpful to explore the architectural design implementations and validity of the proposed architecture. The Snapshots of RTL Schematic of Sigma Delta modulators (without and with applying LMS algorithm) are shown in Fig.8a & Fig.8b.

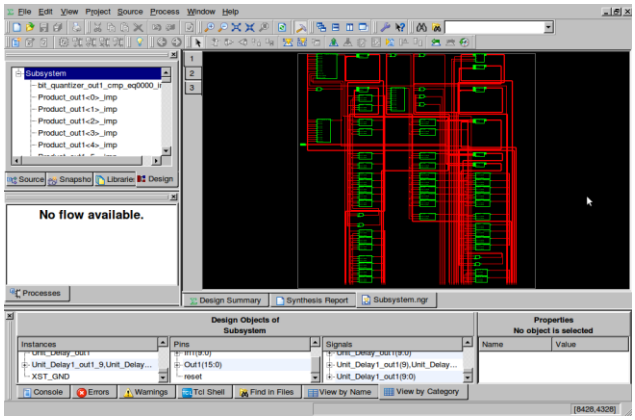

Fig.8b Snapshot of all the components of the Subsystem of the Sigma Delta modulator applying LMS algorithm

5.1 HDL Synthesis Report for Sigma Delta Modulator without LMS

Project File: sigdel_adc.ise
Target Device : xc4vlx25-10-ff668
Product Version: ISE 9.1i
IOs :30
Cell Usage :
#BELS:171;
IO Buffers : 29;
IBUF :12;
OBUF :17;
#DSPs:Nil;
#DSP48:Nil;
Number of Slices: 47 out of 10752 0% ;
Number of bonded IOBs: 30 out of 448 6% ;
Number of 4 input LUTs: : 84 out of 21504 0%;
Number of DSP48s: Nil;
Maximum combinational path delay: 5.630ns;
Total delay: 11.881ns (6.146ns logic, 5.736ns route), (51.7% logic, 48.3% route);
Speed Grade: -10;
CPU : 19.80 / 19.91 s | Elapsed : 22.00 / 24.00 s;
Total memory usage is 225544 kilobytes;

5.2 HDL Synthesis Report for Sigma Delta Modulator Applying LMS Algorithm

Project File: sigdel_lms.ise
Input File Name : "Subsystem1.prj"
Target Device : xc4vlx25-10-ff668
Product Version: ISE 9.1i
IOs :30
Cell Usage :
#BELS:276;
IO Buffers :29;

IBUF : 12;
OBUF : 17;
#DSP48:1;
Number of Slices: 71 out of 10752 0% ;
Number of bonded IOBs: 30 out of 448 6%;
Number of 4 input LUTs: 128 out of 21504 0%;
Number of DSP48s: 1 out of 48 2%;
Maximum combinational path delay:14.103ns;
Total 19.318ns (11.797ns logic, 7.521ns route),(61.1% logic, 38.9% route);
Speed Grade: -10;
CPU : 22.18 / 22.29 s | Elapsed : 34.00 / 36.00 s; Total memory usage is 227472 kilobytes;

6. Analysis on the Synthesis Results

The synthesis reports explore hardware utilization in the both cases. The both architecture use same number of the register, Flip-Flop whereas the normal Sigma-Delta modulator requires less number of Multipliers, adders/Subtractors than the proposed architecture. The sigma delta modulation model without applying LMS algorithm requires no 10x10 bit Multiplier, 4 Adders/Subtractors, no Accumulator 20 Flip Flops and Registers each, 20 I/o buffers, no DSPs, 74 LUTS and zero Ground, VCC and Clock Buffers. Whereas the sigma delta modulation model using LMS Algorithm requires 1 10x10 bit Multiplier, 6 Adders/Subtractors, 1 Accumulator, 20 Flip Flops and Registers each, 29 I/o buffers, 1 DSP, 120 LUTs and 1 Ground, VCC and Clock Buffer each. Though the circuit design of the proposed architecture is more complex than the normal Sigma-Delta Modulator but the proposed scheme is more favorable due to the reduction of noise in the Sigma Delta Modulation with applied LMS algorithm. This provides the high performance Sigma-Delta Modulator. The device utilization summary is also presented in this section.

6.1 Synthesis Results Depicted on the Graph and Comparison Table

Fig. 9a to Fig.9d shows the graphs for the comparison results between Sigma Delta Modulation without applying LMS algorithm and after applying LMS algorithm based on the FPGA Synthesis Reports.

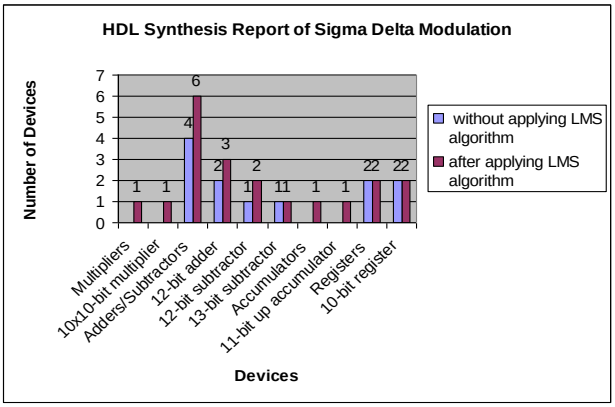

Fig.9a HDL Synthesis Report of Sigma Delta Modulation

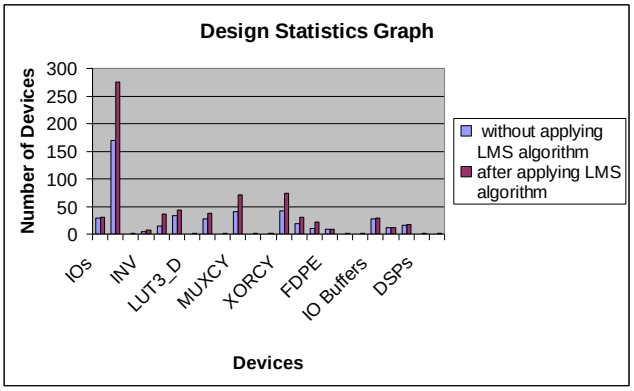

Fig.9b Design Statistics Graph of Sigma Delta Modulation

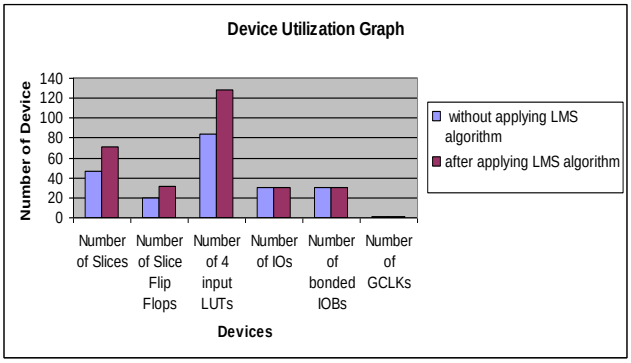

Fig.9c Device Utilization Graph of Sigma Delta Modulation

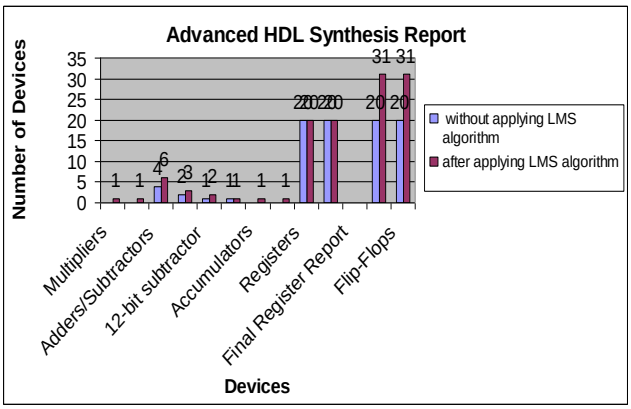

Fig.9d Advanced HDL Synthesis Report of Sigma Delta Modulation

Table 1 Comparison Table

Hardware Components	**Without applying LMS algorithm**	**After applying LMS algorithm**
Advanced HDL Synthesis Report		
Multipliers	NIL	1
10x10-bit multiplier	NIL	1
Adders/Subtractors	4	6
12-bit adder	2	3
12-bit subtractor	1	2
13-bit subtractor	1	1
Accumulators	NIL	1
11-bit up	NIL	1

accumulator		
Registers	20	20
Flip-Flops	20	20
Design Statistics Results		
IOs	29	30
BELS	170	276
GND	0	1
INV	4	7
LUT2	14	36
LUT3	33	44
LUT3_D	NIL	1
LUT4	28	38
LUT4_D	0	1
MUXCY	40	71
MUXF5	0	1
VCC	0	1
XORCY	42	74
FlipFlops/Latches	19	31
FDCE	10	22
FDPE	8	9
Clock Buffers	0	1
BUFGP	0	1
IO Buffers	28	29
IBUF	11	12
OBUF	16	17
DSPs	NIL	1
DSP48	NIL	1
Device utilization summary		
Number of Slices	47 out of 10752	71 out of 10752
Number of Slice Flip Flops	20 out of 21504	31 out of 21504
Number of 4 input LUTs	84 out of 21504	128 out of 21504
Number of IOs	30	30
Number of bonded IOBs	30 out of 48	30 out of 448
Number of GCLKs	1 out of 32	1 out of 32

Conclusions

In this paper, a new architecture has been proposed to reduce noise in a sigma delta modulator. LMS algorithm is applied in the sigma-delta modulator for quantization noise reduction in Sigma Delta modulator. This is useful for performance enhancement of the Sigma-Delta modulator. Here the quantization noise is reduced rapidly as adaptive algorithm is applied in the feedback path of the Sigma Delta modulator. The feedback element also provides stability to the system. This high performance and stable Sigma-Delta modulator is essential for high performance and high speed modern DSP processor design. Matlab and ModelSim simulations validated the above conclusion. In this paper the proposed architecture is also synthesized for FPGA implementation and using this comparative study has been done with the existing Sigma Delta modulator. These results reveal that although the hardware complexity in the proposed architecture is higher than the existing Sigma-Delta modulator but that proposed architecture is more stable and has high performance. Hence this proposed architecture is suitable for performance and speed matching with the modern high speed and high performance DSP processors.

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