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Research Article

Phase Shifted and Level Shifted PWM Based Cascaded Multilevel Inverter Fed Induction Motor Drive

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Abstract

The multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Batteries can be used as the multiple dc voltage sources. This paper focus on phase shifted and level shifted pwm based cascaded multilevel inverter fed induction motor drive. It offer several advantages compared to the conventional 3-phase bridge inverter in terms of lower dv/dt stresses, lower electromagnetic interference, smaller rating and high efficiency. The proposed method has been designed an thirteen level cascaded multilevel inverter by using phase shifted and level shifted pulse width modulation technique and compare the Total harmonic distortion. The selected pattern has been exposed to give superior performance in total harmonics distortion. Simulation and experimental results confirm the feasibility of proposed method.

Keywords: *Multilevel inverter, Cascaded H-bridges, Batteries, PWM Technique, Induction Motor, THD*

1. Introduction

Nowadays, the industry requires power equipment increasingly high, in the megawatt range. The rapid evolution of semiconductor devices manufacturing technologies and the designer's orientation has enabled the development of new structures of converters (inverters) with a great performance compared to conventional structures. So, these new technologies of semiconductor are more suited to high power applications and they enable the design of multilevel inverters. a multilevel converter not only achieves as high power ratings. But also enables the use of renewable energy sources. The commutation of the power switches aggregate these multiple dc sources in order to Achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A Multilevel converter has several advantages over a conventional two-level converter.With the requirement of the quality and efficiency in a high power system and the limitation of high power device switching speed, low switching frequency and small THD.

In the last few years, the necessity of increasing the power quality enhancement in industry has sustained the continuous development of multilevel inverters due to high efficiency with low switching frequency control method. The multilevel inverters improve the AC power quality by performing the power conversion in small voltage steps resulted in lower harmonics. The output voltage on the AC side can take several discrete levels of equal magnitude. The harmonic content of this output voltage waveform is greatly reduced, a smaller filter size and a lower EMI, if compared with a two level voltage waveform. Several topologies for multi-level inverters have been proposed over the years the most popular being the diode clamped, flying capacitor and cascaded H-bridge structures. One aspect which sets the cascaded H-bridge apart from other multi-level inverters is the capability of utilizing different DC voltages on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher frequency Inverters.

The use of a multilevel inverter to control the frequency, voltage output (including phase angle), and real and reactive power flow at a dc/ac interface provides significant opportunities in the control of distributed power systems.

2. Cascaded multilevel inverter

a) Basic principle

The general function of the multilevel inverter is to synthesize a desired ac voltage from several levels of dc voltages. For this reason, multilevel inverters are ideal for

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connecting either in series or in parallel an ac grid with renewable energy sources such as photo-voltaic or fuel cells or with energy storage devices such as capacitors or batteries. An alternate method of cascading inverters involves series connection of two, three-phase inverters through the neutral point of the load. Past research has shown this concept for cascading two-level inverters and multi-level inverters. An advantage of this approach is that isolated sources are not required for each phase. It should be noted that cascaded inverter systems can be considered from a number of different viewpoints. Considering the cascaded inverter to be one unit, it can be seen that a higher number of voltage levels are available for a given number of semiconductor devices. Multilevel power inverters employ power semiconductor switches in the inverter to select one or more of multiple dc voltage sources to create staircase voltage waveform at the inverter output. Capacitors batteries or renewable energy voltage sources can be used as a DC voltage sources. The control of the power switches permits the addition of the multiple DC sources in order to achieve desired staircase waveform at the high power output. The below Fig.1 represents the schematic diagram of cascaded H-bridge Multilevel Inverter.

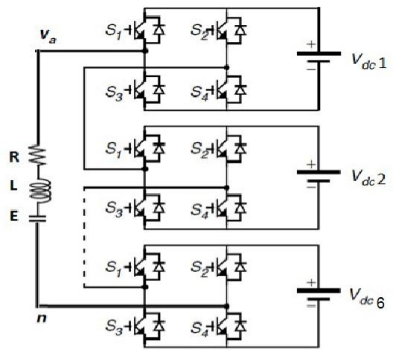

Fig.1. Cascaded 13-level Multilevel Inverter

This paper proposes phase shifted and level shifted PWM based cascaded multilevel schemes is discussed. This scheme does not require any modification in the carrier or modulating signal. It has advantage or superiority over other previous works. The modeling of in this paper highlights significance of a thirteen level cascaded multilevel inverter applied to two different conditions, those are connected to induction motor drive.

The proposed method has been designed an Thirteen-level cascaded multilevel inverter, which has six single-phase full-bridge inverter connected in series, it has produce the desired thirteen-level phase voltage. Phase voltage wave form for a thirteen-level cascaded multilevel inverter with six SDCSs and six full bridges. The phase voltage

$$V_{an} = V_{a1} + V_{a2} + V_{a3} + V_{a4} + V_{a5} + V_{a6}$$

The Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4\,Vdc}{\pi}\sum_n[\cos(n\theta 1) + \cos(n\theta 2) + \ldots$$

$$\ldots + \cos(n\theta s)]\; X\; \frac{\sin(n\omega t)}{n},$$

Where n =1, 3, 5, 7…

The magnitudes of the Fourier coefficients when normalized with respect to Vdc are as follows.

$$H(n) = \frac{4}{\pi n}[\cos(n\theta 1) + \cos(n\theta 2) + \ldots. + \cos(n\theta s)]\,,$$

Where n =1, 3, 5, 7….

3. Multilevel Inverter Operation

An overview of the system is shown in Figure1. The core component of this inverter design is the four-switch combination shown in Figure 1. By connecting the DC source to the AC output by different combinations of the four switches, S1, S2, S3, and S4, three different voltage output levels can be generated for each DC source. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. A cascaded inverter with N input sources will provide (2N+1) levels to synthesize the AC output waveform.

4. Switching Pattern Scheme

In this paper, control technique of phase shifted (PS-PWM) and level shifted (LS-PWM) pulse width modulation strategy is employed. The two pwm techniques are,

4.1 Phase Shifted PWM (PSCPWM)

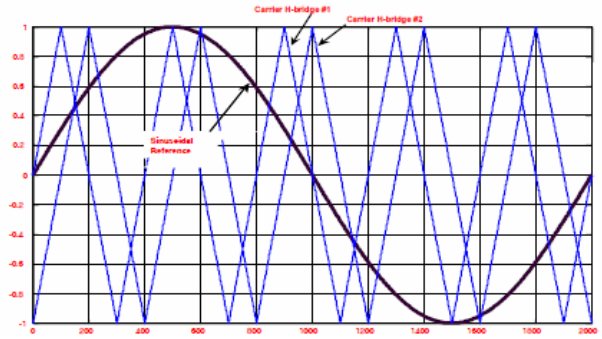

Fig. 2 Phase Shifted Carrier PWM

In psc pwm all the triangular carriers have the same frequency and same peak-peak amplitude .but there is a phase shift between any two adjacent carrier waves.For m Voltage levels (m-1) carrier signals are required and they are phase shifted with an angle of θ=(360°/m-1).The gate signals are generated with proper comparison of carrier wave and modulating signal .

4.2 Level shifted PWM (LSCPWM

For carriers signals, the time values of each carrier waves are set to [0 1/600 1/300] while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are

transmitted to the IGBT. This technique is divided into 3 types,

In Phase disposition (IPD)

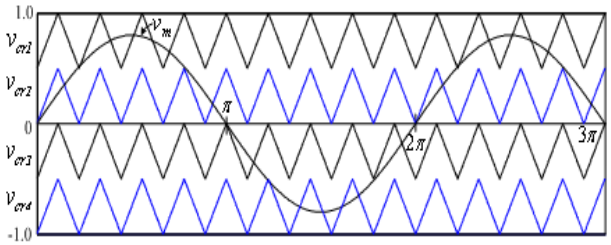

Fig.3 in phase disposition

All the carrier signals are in phase.

Phase opposition disposition (POD)

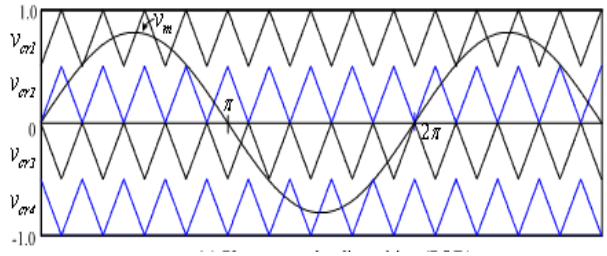

Fig.4 phase opposition disposition

All the carriers above zero reference are in phase but in opposition with those are below zero reference.

Alternate phase opposition disposition (APOD)

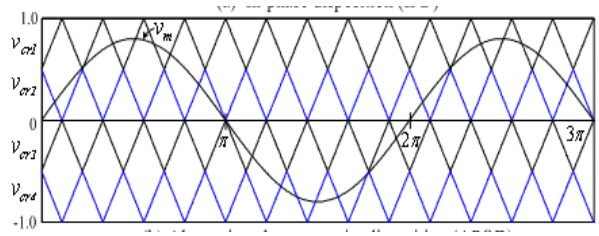

Fig.5 Alternate phase opposition disposition

The modulating signal of each phase is displaced from each other by 120°. All the carrier signals have same frequency Fc and amplitude Ac while the modulating signal has a frequency of fm and amplitude of Am. The fc should be in integer the multiples of fm with three-times. This is required for all the modulating signal of all the three phases see the same carriers, as they are 120° apart. The carrier waves and the modulating signals are compared and the output of the comparator defines the output in the positive half cycle the comparator output will have the value high, if the amplitude of the modulating signal is greater than that of the carrier wave and zero otherwise. Similarly for the negative half cycle, if the modulating signal is lower than the carrier wave the output of the comparator is high and zero otherwise.

In the Thirteen-level cascaded multilevel inverter each carrier waveform and sine waveform are compared individually. The simulation model of switching pulses generation is shown in fig 6. The each comparator output is given to cascaded multilevel inverter switching devices. As the comparator output is directly given to S1and S4. In the Thirteen-level cascaded multilevel inverter twelve carrier waveforms and a sine waveform are compared with individual comparator. This comparator output is given to Sj where j= 1 to 12, using this manner inverter obtained Thirteen levels phase voltage.

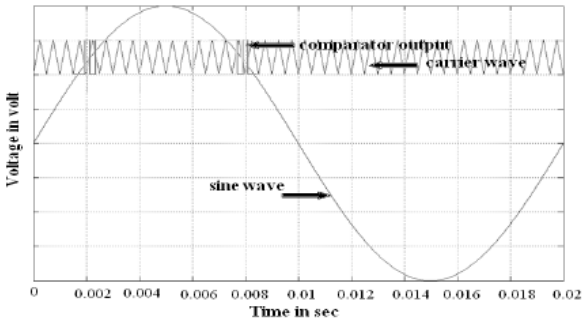

Fig.6 Sinusoidal and Carrier Wave Comparison

5. Matlab Modeling and Simulation Results

In that the simulation is carried out of two cases:

i) Cascaded Multi level inverter fed Induction Motor drive with phase shifted PWM technique
ii) Cascaded Multi level inverter fed Induction Motor drive with level shifted PWM technique
Case i: Cascaded Multi level inverter fed Induction Motor drive with phase shifted PWM technique,

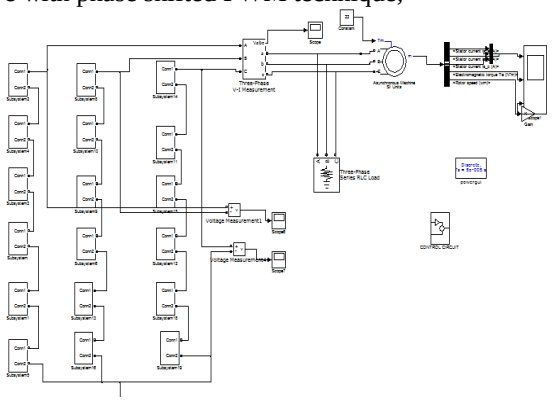

Fig.7 13-level Cascaded Multilevel Inverter Fed Induction Motor drive with phase shifted PWM technique

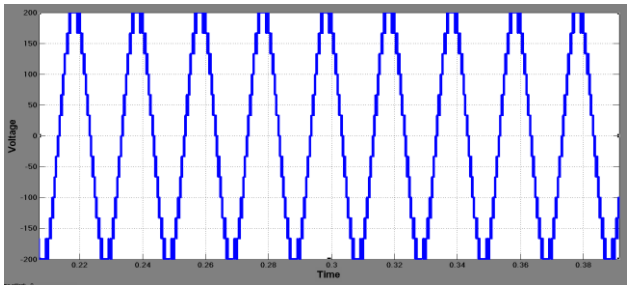

Fig.8 phase voltage of cascaded Multilevel Inverter

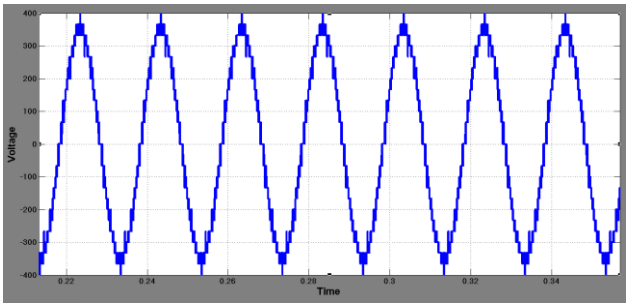

Fig. 9 Line voltage of Cascaded Multilevel Inverter

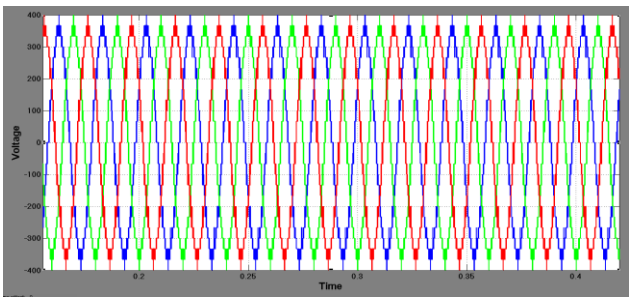

Fig 103-phase Line voltage of Cascaded Multilevel inverter

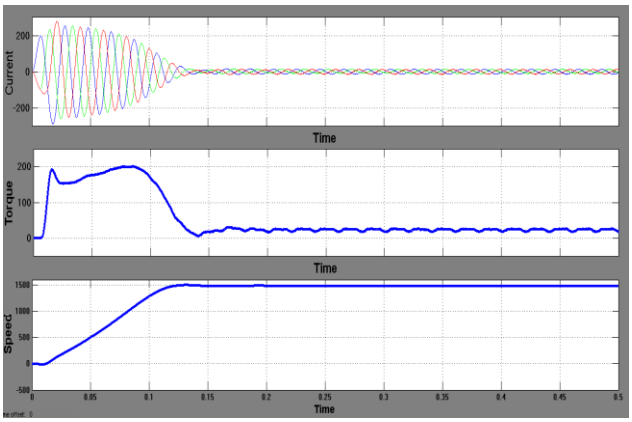

Fig.11 Stator current, Torque and speed characteristics of 3-phase Induction Motor Drive

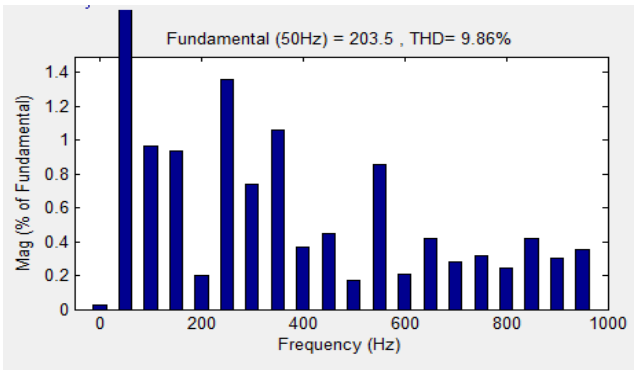

Fig. 12 THD Analysis of 13-level Cascaded Multilevel Inverter with phase shifted PWM

Case ii: Cascaded MLI Fed Induction Motor Drive with Level shifted PWM technique.

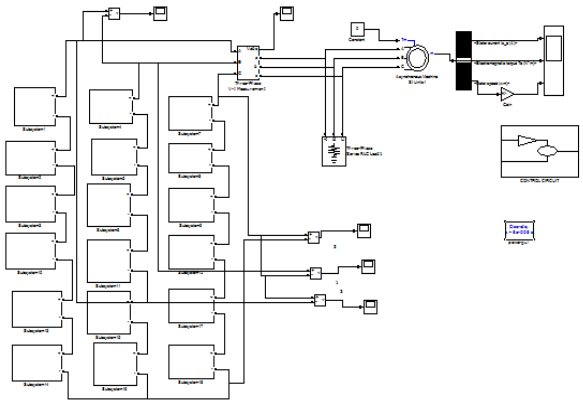

Fig. 13 Cascaded MLI Fed Induction Motor Drive with Level shifted PWM

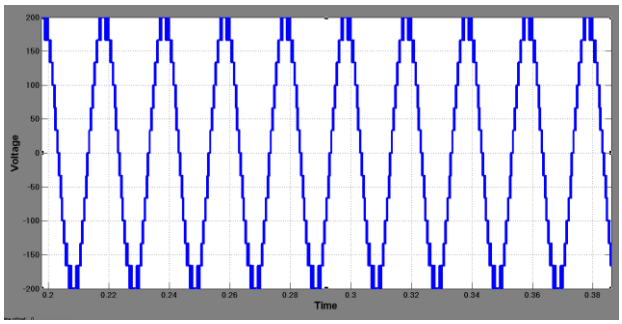

Fig.14 phase voltage of Cascaded Multilevel Inverter

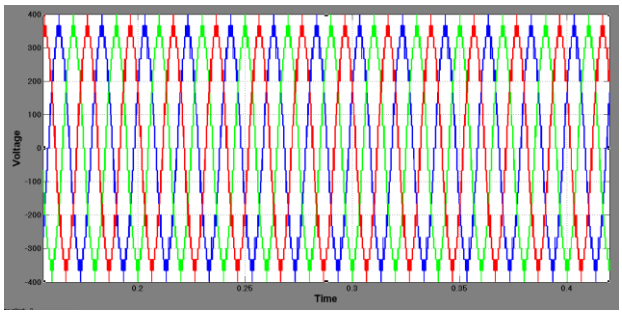

Fig.15 3-phase line voltage of cascaded Multi level Inverter

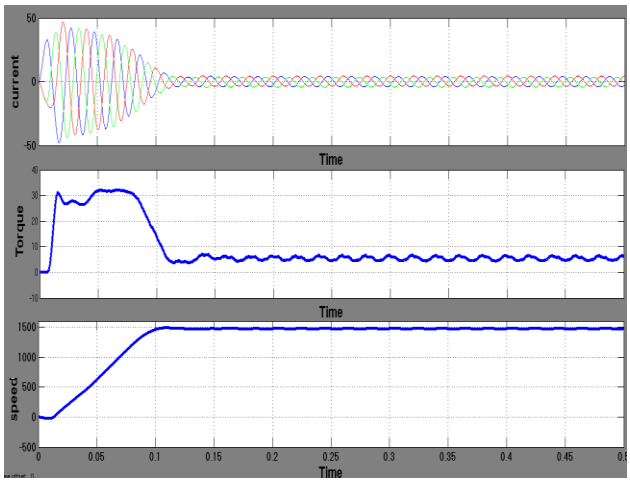

Fig.16 Induction Motor characteristics

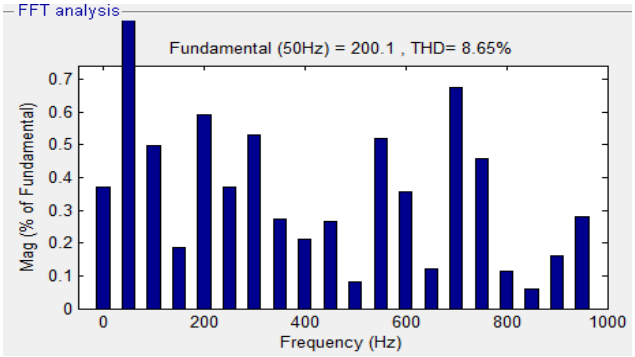

Fig.17 THD Analysis of 13-level Cascaded MLI with level shifted PWM technique

Comparison of THD

Control Technique	**13-Level THD**	
	Phase voltage	Line voltage
Phase shifted PWM	**9.86%**	**8.15%**
Level shifted PWM	**8.65%**	**7.05%**

In That the THD of 13-Level Multilevel inverter with phase shifted PWM has 9.86% and Level shifted PWM has 8.65%.

Conclusion

In this paper, 13-Level Cascaded multilevel inverter has been designed with phase shifted and level shifted PWM techniques. And compare the total harmonic distortion of 13 –level inverter for both the PWM techniques. This technique is used to improve the level of the inverter and extends the design flexibility and reduces the harmonics. Multilevel inverter is obtain output with high resolution. When the number of level increase total harmonic distortion should be decreased. The 13-level Cascaded multilevel inverters with induction motor characteristics are verified through simulation results by using MATLAB. The simulation results are give better quality of stator currents with low harmonics, and motor characteristics.

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