

Research Article

A Novel Five-level Inverter topology Applied to Four Pole Induction Motor Drive with Single DC Link

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Abstract

Multi-level inverter technology has emerged recently as a very important alternative in the area of high-power high-voltage energy control. So multi-level inverters have been widely used for high-power high-voltage drive applications. Due to higher number of sources, lower EMI, lower % THD in output voltage and less stress on insulation, they are widely used. In this paper an optimized five-level inverter topology is proposed for a four pole induction motor drive. To minimize the common mode currents a Sine-Triangle Pulse Width Modulation is used in the proposed topology. Thereby the first dominant harmonics and triplen harmonics shifted near to the switching frequency, which will have a less impact on the motor phase currents. Since the dominant harmonics are less in the proposed topology, it gives almost sinusoidal output voltage which will improve the efficiency of the drive system. The simulation results based on Matlab/Simulink are discussed in detail in this paper.

Keywords: Five-level inverter, Induction motor, Sine triangle, PWM.

1. Introduction

The conventional voltage source inverters produce an output voltage at the poles with levels $\pm V_{dc}/2$, where V_{dc} is the dc-link voltage, are known as the two-level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high-switching frequency along with various pulse-width modulation (PWM) strategies (Muhammad H. Rashid,2003). In high-power and high-voltage applications, these two-level inverters however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings. Moreover, the semiconductor switching devices should be used in such a manner as to avoid problems associated with their series parallel combinations that are necessary to obtain capability of handling high-voltages and currents. The multi-level inverter includes an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions (Muhammad H. Rashid , 2003).In this paper a five-level inverter topology is proposed for the

induction motor drive by using four conventional two-level inverters only, with the advantage of two identical voltages profile winding coils of four pole induction motor which will be explained in detail in the next section.

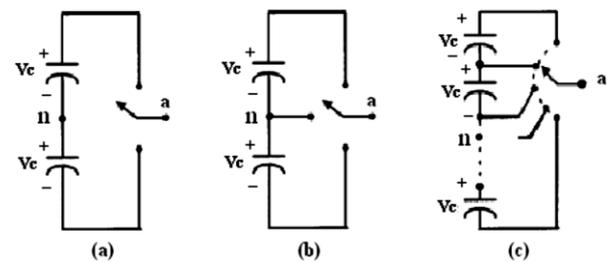


Fig 1 One leg of inverter with (a) two-levels (b) three-levels and (c) n-levels

The identical voltage profile winding coils are disconnected and each part of the winding is fed with two two-level inverters from both sides. Thereby four two-level inverters are used to generate five voltage levels on motor phase windings. All two-level inverters are fed with single DC link with the magnitude $\frac{V_{dc}}{4}$. The proposed topology uses sine-triangle PWM to generate the pulses for the switches of each inverter which will also minimize the common mode currents circulating in the motor phase windings because of the common DC link.

2. Dynamic Modelling of Induction Motor

In a conventional four pole induction motor, there are two

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sets of identical voltage profile windings will be present in the total phase winding (M. G. Say , 1990). These two windings are connected in series as shown in fig. 2(a). For the proposed inverter these two identical voltage profile winding coils are disconnected, and the available four terminals are taken out, like shown in the fig.2 (b). Since these two windings are separated equally, stator resistance, Stator leakage inductance and the magnetizing inductance of each identical voltage profile windings are equal to the half of the normal induction motor shown in fig.2 (a). The voltage equation for the stator winding is given by common dc link.

$$V_{a1}-V_{a2}=(\frac{r_s}{2}) * i_{as}+(\frac{l_{ss}}{2}) * i_{as}-(\frac{1}{2}) * \frac{L_m}{2} * i_{bs}-\frac{1}{2} * \frac{L_m}{2} * i_{cs} \quad (1)$$

$$V_{a3}-V_{a4}=(\frac{r_s}{2}) * i_{as}+(\frac{l_{ss}}{2}) * i_{as}-(\frac{1}{2}) * \frac{L_m}{2} * i_{bs}-\frac{1}{2} * \frac{L_m}{2} * i_{cs} \quad (2)$$

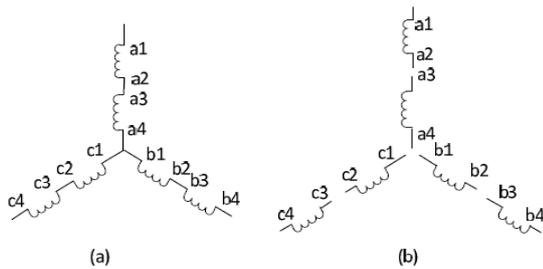


Fig. 2: Induction Motor stator winding: (a) General arrangement (b) Arrangement for the proposed inverter

The effective voltage across the stator winding is the sum of the voltages across the two individual windings.

$$V_{as} = (V_{a1}-V_{a2})+(V_{a3}-V_{a4}) \quad (3)$$

The motor phase voltage can be achieved by substituting equations (1) and (2) in (3)

$$V_{as}=(r_s) * i_{as}+l_{ss} * i_{as}-\frac{1}{2} * L_m * i_{bs}-\frac{1}{2} * L_m * i_{cs} \quad (4)$$

Similarly voltage equation for the remaining phases are

$$V_{bs} = (r_s) * i_{bs}+l_{ss} * i_{bs}-\frac{1}{2} * L_m * i_{as}-\frac{1}{2} * L_m * i_{cs} \quad (5)$$

$$V_{cs} = (r_s) * i_{cs}+l_{ss} * i_{cs}-\frac{1}{2} * L_m * i_{as}-\frac{1}{2} * L_m * i_{bs} \quad (6)$$

Voltage equations in dq0 frame can be solved from the basic equations of induction motor.

$$V_{qs}=r_s * i_{qs}+\omega * \lambda_{ds}+\rho * \lambda_{qs}$$

$$V_{ds}=r_s * i_{ds}+\omega * \lambda_{qs}+\rho * \lambda_{ds}$$

$$V_{os}=r_s * i_{os}+\rho * \lambda_{os}$$

$$V_{qr} = r_r * i_{qr}+(\omega - \omega_r) * \lambda_{dr}+\rho * \lambda_{qr}$$

$$V_{dr} = r_r * i_{dr}+(\omega - \omega_r) * \lambda_{qr}+\rho * \lambda_{dr}$$

$$V_{or}=r_r * i_{or}+\rho * \lambda_{or}$$

Flux linkages are as follows

$$\lambda_{qs}=L_{ss} * i_{qs}+L_M * i_{qr}$$

$$\lambda_{ds}=L_{ss} * i_{ds}+L_M * i_{dr}$$

$$\lambda_{os}=L_{1s} * i_{os}$$

$$\lambda_{qr}=L_{rr} * i_{qr}+L_M * i_{qs}$$

$$\lambda_{dr}=L_{rr} * i_{dr}+L_M * i_{ds}$$

$$\lambda_{or}=L_{1r} * i_{or}$$

The expression for the electromagnetic torque in terms of dq0 axis currents is

$$T_e=\frac{3}{2} * \frac{P}{2} * L_M * (i_{qs} * i_{dr}+i_{ds} * i_{qr}) \quad (7)$$

Rotor speed in terms of Torque is

$$\frac{d}{dt} \omega_e = \left(\frac{P}{2 * J}\right) * (T_e - T_L) \quad (8)$$

Where

d: direct axis,

q: quadrature axis,

s: stator variable,

r: rotor variable,

V_{ds}, V_{qs} : q and d-axis stator voltages,

V_{dr}, V_{qr} : q and d-axis rotor voltages,

r_r : Rotor resistance,

Vr_s : Stator resistance,

L1s: stator leakage inductance,

L1r : rotor leakage inductance,

i_{qs}, i_{ds} : q and d-axis stator currents,

i_{qr}, i_{dr} : q and d-axis rotor currents,

p: number of poles,

J: moment of inertia,

T_e : electrical output torque,

T_L : load torque.

From the equations (4), (5),(6) it can be observed that there is no difference between the normal induction motor shown in fig.2 (a) and the disconnected (Identical voltage profile windings) motor shown in fig.2 (b).

3. Proposed Five-Level Inverter Topology

The five-level inverter topology has proposed for the four pole induction motor drive. The two identical voltage profile winding coils are disconnected, total four available terminals were taken out and fed with four two-level inverters and it is shown in fig. 3. These four two-level inverters were supplied with a single DC source having magnitude $\frac{V_{dc}}{4}$. In the fig.3 S11 to S16 are the switches of the first inverter, S21 to S26 are the switches of the second inverter, S31 to S36 are the switches of the third inverter, S41 to S46 are the switches of the fourth inverter. The blocking voltage of all these switches is $\frac{V_{dc}}{4}$ (S11, S12), (S13, S14), (S15, S16) are the complementary switches of the first inverter (that is if S11 is on S12 will be off) and it is same to remaining three inverters. The switches S1 to S6 are the auxiliary switches needed to isolate the middle two inverters (invert-2 and invert-3 as shown in fig.2) during the voltage levels of $-\frac{V_{dc}}{4}, 0, \frac{V_{dc}}{4}$ (K. Sivakumar , 2010). If the switches S1 to S6 are shorted, then unequal voltage distribution will happen across the motor phase windings (two identical voltage profile windings) which in turn causes unequal flux distribution and is explained clearly in (M. G. Say , 1990). The possible switching combinations available for A-phase for generating five voltage levels $(-\frac{V_{dc}}{2}, -\frac{V_{dc}}{4}, 0, \frac{V_{dc}}{2}, \frac{V_{dc}}{4})$ across motor terminals is shown in the Table-I. The proposed five-level inverter topology is compared with conventional topologies (in terms of the switching devices, capacitor

banks, and isolated voltage sources), and is presented in the table-II.

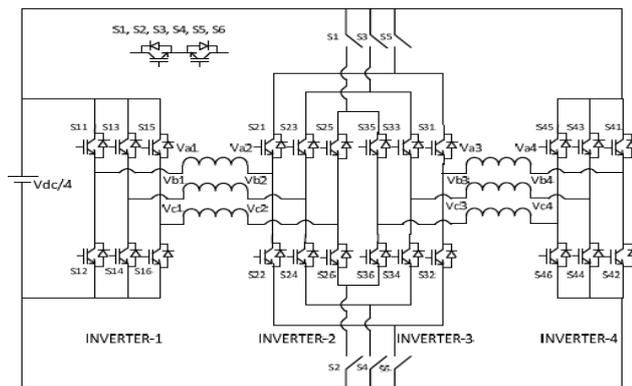


Fig. 3: Proposed five-level inverter

Table –I Possible switching combinations to generate five voltage levels

Voltage Magnitude	S ₁₁	S ₂₁	S ₃₁	S ₄₁	S _{A1} S _{A1'}	S _{A2} S _{A2'}
$+\frac{V_{dc}}{2}$	ON	OFF	ON	OFF	ON	ON
$+\frac{V_{dc}}{4}$	ON	ON	ON	OFF	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF
	ON	OFF	OFF	ON	OFF	OFF
	ON	ON	ON	ON	OFF	OFF
	OFF	ON	ON	OFF	OFF	OFF
$-\frac{V_{dc}}{4}$	OFF	OFF	OFF	ON	OFF	OFF
$-\frac{V_{dc}}{2}$	OFF	ON	ON	ON	OFF	OFF

Table-II Comparison between the conventional topologies with proposed one

	NPC inverte r	FC inverte r	HB inverte r	Proposed inverter
switches*	24	24	24	24
Clamping Diodes	$3 * \frac{V_{dc}}{4}$	6	0	0
	$\frac{V_{dc}}{2}$	6	0	0
	$\frac{V_{dc}}{4}$	6	0	0
Isolated voltage sources	1* (V _{dc})	1* (V _{dc})	6* ($\frac{V_{dc}}{4}$)	1* ($\frac{V_{dc}}{4}$)
Capacitor Banks*	4	18	0	0
Bi-directional switches	0	0	0	6 ($\frac{V_{dc}}{8}$)

Switches* = Switches (with a voltage rating of $\frac{V_{dc}}{4}$)
 Capacitor Banks* = Number of capacitor banks (with a voltage rating of $\frac{V_{dc}}{4}$)

It can be observed that the number of main (inverter) switches required is the same for all the topologies. But the proposed topology does not require any additional clamping diodes whereas the NPC does require six diodes

of rating $3 * (\frac{V_{dc}}{4})$, six diodes of rating $\frac{V_{dc}}{2}$ and six diodes of rating $\frac{V_{dc}}{4}$. The proposed topology requires one DC source having magnitude $\frac{V_{dc}}{4}$ but H-Bridge inverter require six voltage source of magnitude $\frac{V_{dc}}{4}$ and NPC, FC require one DC source having magnitude Vdc.

4. Sine Triangle Pulse Width Modulation

A sine-triangle PWM for the multi-level inverters is used to generate the gating pulses for the proposed inverter topology (McGrath et al , 2002). In the Sine triangle Pulse width modulation for generating five voltage levels on motor phase winding, it requires one modulating signal and four carrier signals (McGrath et al , 2002) as shown in the fig.4. The frequency of the modulating signal (sine wave) is maximum of 50HZ, whereas the carrier signal frequency is kept at constant at 2 KHZ.

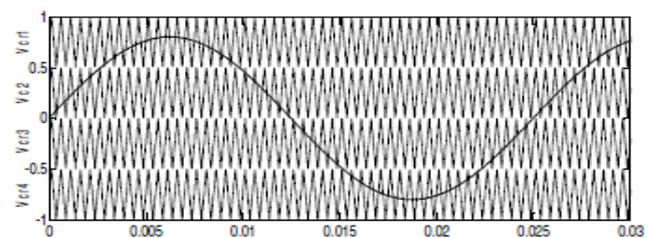


Fig 4 Modulating and carrier waves for generating pulses in SPWM

The patron followed for generating the five voltage levels for one phase is shown in the Table-3

Table-III Comparison of carrier and modulating signals corresponding to the output voltage

Comparison between Modulating and Carrier signals	Output Voltage Level
$V_M > V_{cr1}$	$+\frac{V_{dc}}{2}$
$V_{cr2} < V_M < V_{cr1}$	$+\frac{V_{dc}}{4}$
$V_{cr3} < V_M < V_{cr2}$	0
$V_{cr4} < V_M < V_{cr3}$	$-\frac{V_{dc}}{4}$
$V_M < V_{cr4}$	$-\frac{V_{dc}}{2}$

When $V_M > V_{cr1}$ switches S11, S22, S31, S42 of Phase-A are conducting and it is giving the output voltage $+V_{dc}/2$. $V_{cr2} < V_M < V_{cr1}$ switches S11, S22, S32, S42 of Phase-A are Conducting and it is giving the output voltage $+V_{dc}/4$. $V_{cr3} < V_M < V_{cr2}$ switches S12, S22, S32, S42 of Phase-A are Conducting and it is giving the output voltage 0. $V_{cr4} < V_M < V_{cr3}$ switches S11, S22, S32, S41 of Phase-A are conducting and it is giving the output voltage $-V_{dc}/4$. $V_M < V_{cr4}$ switches S12, S21, S32, S41 of Phase-A are Conducting and it is giving the output voltage $-V_{dc}/2$. Many switching combinations are possible (which are shown in Table-I) but above stated switching combinations are used to minimize the switching transitions from one voltage level to other voltage level.

5. Matlab Modeling and Simulation Results

The propose five-level inverter is simulated with induction motor. The gating pulses, to the switches of the proposed five-level inverter, were generated with sin-triangle pulse width modulation. The four terminals (per phase) of the induction motor connected to four inverters with single DC link, having magnitude $V_{dc}/4$. Here simulation is carried out in different cases 1). Proposed Five Level Inverter Topology 2). Proposed Five Level Inverter Topology with Induction Machine Drive.

Case 1: Proposed Five Level Inverter Topology

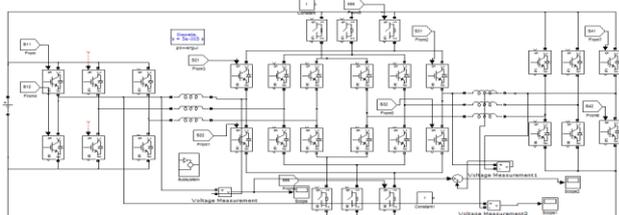


Fig.5 Matlab/Simulink Model of Proposed Five Level Inverter Topology

Fig.5 shows the Matlab/Simulink Model of Proposed Five Level Inverter Topology using Matlab/Simulink Platform.

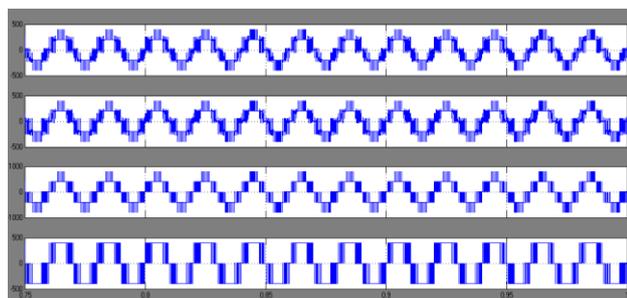


Fig.6 Top trace is the voltage between the points A1 and A2. Second Top trace is the voltage between the points A3 and A4. Third Top trace is the effective voltage across the motor phase winding.

Fig.6 shows the Top trace is the voltage between the points A1 and A2. Second Top trace is the voltage between the points A3 and A4. Third Top trace is the effective voltage across the motor phase winding.

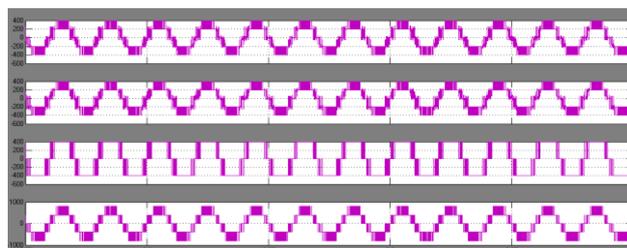


Fig.7 Top trace is the voltage between the points A1 and A2. Second Top trace is the voltage between the points A3 and A4. Third Top trace is the effective voltage across the motor phase winding.

Fig.7 shows the Top trace is the voltage between the points A1 and A2. Second Top trace is the voltage between the points A3 and A4. Third Top trace is the effective voltage across the motor phase winding.

Case 2: Proposed Five Level Inverter Topology with Induction Machine Drive

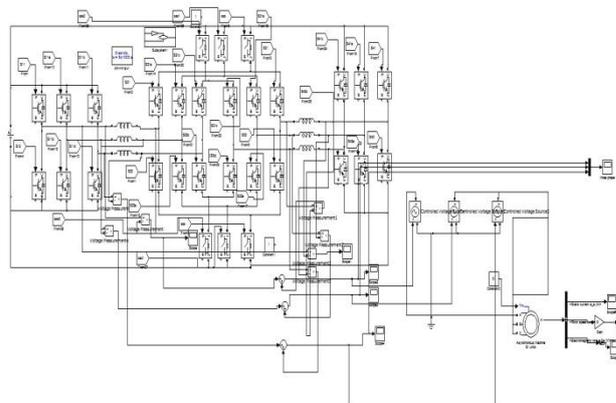


Fig.8 Matlab/Simulink Model of Proposed Five Level Inverter Topology with Induction Machine Drive

Fig.8 shows the Matlab/Simulink Model of Proposed Five Level Inverter Topology with Induction Machine Drive using Matlab/Simulink Platform.

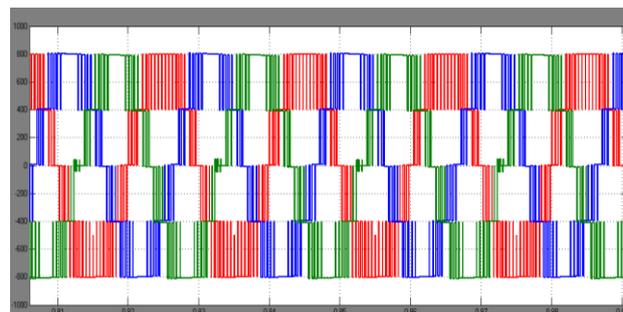


Fig.9 Three Phase Five Level Output Voltage

Fig.9 shows the Three Phase Five Level Output Voltage of Proposed Five Level Inverter Topology with Induction Machine Drive.

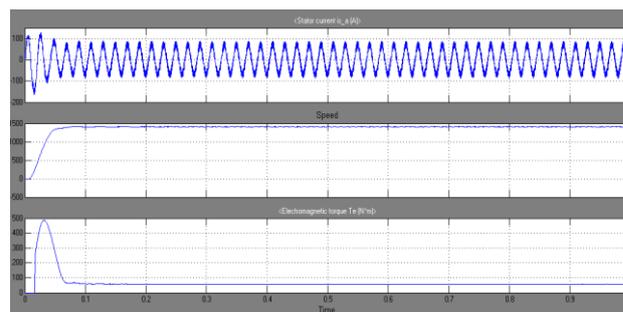


Fig.10 Stator Current, Speed, Electromagnetic Torque

Fig.10 shows the Stator Current, Speed, and Electromagnetic Torque of Proposed Five Level Inverter Topology with Induction Machine Drive.

Conclusion

Multilevel voltage source converters are emerging as a new breed of power converter options for high-power applications. In this paper an optimized five-level inverter topology is presented for a four pole induction motor drive. This topology has developed by using the advantage of two identical voltage profile winding coils per phase in a four pole induction motor. The identical voltage profile winding coils are disconnected and each part of the winding is fed with two two-level inverters from both sides. Thereby four two-level inverters are required to generate five voltage levels. All two-level inverters are fed with single DC link with the magnitude $V_{dc}/4$. The proposed topology is simulated in MATLAB (Simulink). From the results it can be observed that the common mode currents generated because of the single DC link are minimized. The proposed topology does not require any major design modifications of induction motor. An important feature of this topology is that if the middle inverter switches (inverter-2 and inverter-3) are failed, it will be operated as a three-level inverter up to the modulation index 0.5. Thereby the reliability of the system increases. Finally a three phase model with induction machine drive of the proposed circuit is shown for evaluating the drive performance and simulation results are presented.

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