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Research Article

Implementation of 16X16 SRAM Memory Array using 180nm Technology

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Abstract

Static Random access memory (SRAM) are useful building blocks in many applications such as a data storage embedded applications, cache memories, microprocessors. Large SRAM arrays that are widely used as cache memory in microprocessors and application-specific integrated circuits can occupy a significant portion of the die area. For high density circuits such as SRAM arrays, which are projected to occupy more than 90% of the SoC area in the next 10 years. In an attempt to optimize the performance of such chips, large arrays of fast SRAM help to boost the system performance. However, the area impact of incorporating large SRAM arrays into a chip directly translates into a higher chip cost. Balancing these requirements is driving the effort to minimize the footprint of SRAM cells. As a result, millions of minimum-size SRAM cells are tightly packed making SRAM arrays the densest circuitry on a chip. In this paper an effort is made to design 16X16 SRAM memory array on 180nm technology. For high-speed memory applications such as cache, a SRAM is often used. Access time, speed, and power consumption are the three key parameters for an SRAM memory design(SRAM). The integrated SRAM is operated with analog input voltage of 0 to 1.8v. The 16x16 SRAM memory has been designed, implemented & analysed in standard UMC180nm technology library using Cadence tool.

Keywords: *SRAM, Access time, Cadence, power consumption, UMC180*

1. Introduction

With the rapid growth of modern communications and signal processing systems, handheld wireless computers and consumer electronics are becoming increasingly popular.. SOC designs have made possible substantial cost and form factor reductions, in part since they integrate crucial memory components with digital computing and signal processing circuits on the same die which occupies70% of the space. The SRAM is major component only occupy larger area of the chip die and for SOC designs, the technology selection and system design choices are mainly driven by digital circuit requirements.The demand for static random-access memory (SRAM) is increasing with large use of SRAM in mobile products, System On-Chip (SoC) and high-performance VLSI circuits. 70% of the area in System On-Chip (SoC) is consumed by SRAM memory. SRAM is significant component used for the cache memory in microprocessors, main frame computers, engineering workstations and memory in hand-held devices due to high speed and low power consumption.

The Cadence tool (version 5.14) is used to design SRAM. The technology file attached is UMC180 (United Microelectronics Limited) which is industry Standard and directly given to a fabrication unit for fabrication.

Low power SRAM array implementation is used to demonstrate the feasibility of low power memory design. SRAM array is constructed using the basic 6T SRAM cell. The paper aims to propose the design for 32 bytes(256 bits) memory using Schematic Editor Virtuoso. Peripheral circuits like Row Decoder, Pre-charge Circuit, Write driver circuit, bit cell and Sense Amplifier are to be designed and implemented. The project aims to implement the memory and demonstrate successful write and read operations. In this paper, a SRAM memory array design is proposed that is a true low power and high speed which can be represented by lower access time.

2. Background

The paper on “A single ended 6T SRAM cell design for ultra low voltage applications” in IEICE 2008, pg 750-755, September25,2008 by JawarSingh, DhirajK.Pradhan, Simon Hollis, Saraju P. Mohanty discuss about the advancement of technology, and also about the memory cell. This evolution of technology provides much faster transistors with smaller sizes, making it possible to have very high clock rate in digital circuits. In the end, it leads us to design a very high speed as well as systems with small die area called System on a chip (SoC), with a smaller number of chips using increased integration level. Semiconductor memory arrays are capable of storing

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large quantities of digital information which are essential to all digital systems. The amount of memory required in a particular system depends on the type of the application, in general, the number of transistors for the information(data) storage function is much larger than the number of transistors used for logic operations and others. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development toward more compact design rules and, consequently, toward higher data storage densities. Thus, the maximum realizable data storage capacity of single-chip semiconductor memory arrays approximately doubles every two years. On-chip memory arrays are the most primary component used in many subsystems in many VLSI circuits, and commercially available single-chip read/write memories. The memory capacity has reached 1gigabits (1Gb).The trend toward higher memory density and larger storage capacity will continue to push the leading edge of digital system design. Section III discuss about the SRAM architecture, in the mean while Section IV about its Implementation. Section V, VI describes the experimental results and Conclusion respectively.

3. SRAM architecture

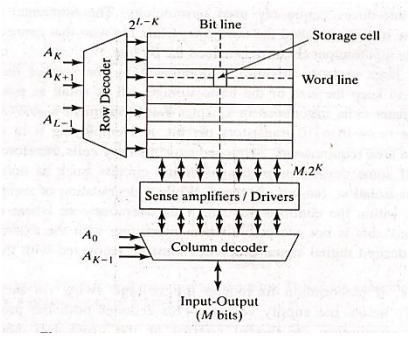

Fig.1: General SRAM array structure.

The above Fig.1.,shows a typical SRAM block diagram. SRAMs can be organized as bit-oriented or word-oriented. In a bit-oriented SRAM, each address accesses a single bit, whereas in a word-oriented memory, each address addresses a word of *n* bits (where the popular values of n include 8, 16, 32 or 64). Column decoders or column MUXs (YMUXs) addressed by Y address bits allow sharing of a single sense amplifier among 2,4or more columns. An SRAM cell must be designed such that it provides a non-destructive read operation and a reliable write operation. These two requirements impose contradicting requirements on SRAM cell transistor sizing. SRAM cell transistor ratios that must be observed for successful read and write. The main SRAM building blocks are as follows

- SRAM cell.
- Pre-Charge Circuit.
- Write Driver Circuit.
- Sense Amplifier.
- Row decoder.

4. Design and implementation

This section deals with implementation of five components as mentioned in section III.

4.1 The SRAM cell

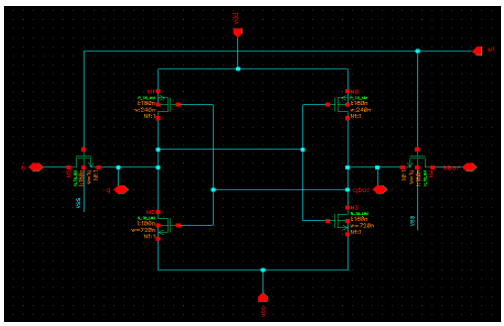

Fig. 2: Schematic of SRAM cell.

SRAM cell design considerations are important for a number of reasons. Firstly, the design of an SRAM cell is key to ensure stable and robust SRAM operation. Secondly, owing to continuous drive to enhance the on-chip storage capacity, the SRAM designers are motivated to increase the packing density. Therefore, an SRAM cell must be as small as possible while meeting the stability, speed, power and yield constraints. An SRAM cell is the key SRAM component storing binary information. It has both read and write capabilities. The word line defines operational modes. When wl=’0’ both access transistor’s are off and cell is isolated.To perform read or write operation the word line is brought upto a value of ‘1’which turns on both access transistors. A typical SRAM cell uses two cross-coupled inverters forming a latch and access transistors. Access transistors enable access to the cell during read and write operations and provide cell isolation during the not-accessed state. An SRAM cell is designed to provide non-destructive read access, write capability and data storage (or data retention)for as long as cell is powered. The width and length of pmos transistor is 240n and 180n respectively. The width and length of nmos transistor is 720nn and 180n respectively. The width and length of access transistor is 1u and 180n respectively.

4.2 The Pre-Charge Circuit

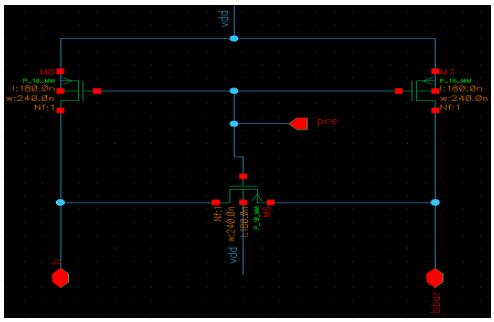

Fig. 3: Schematic of Pre-Charge circuit.

The pre charge circuit is one of the essential component used in SRAM. The function of SRAM is to charge the bit and bitbar lines to Vdd=1.8v.The pre charge circuit enables the bit lines to be charged high at all times except during read and write operation. The width required for PMOS is minimum i.e 240n and length is fixed to 180nm. For each column single pre charge circuit is used.

4.3 Write Driver Circuit

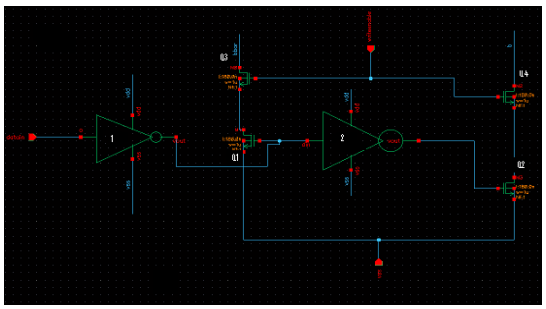

Fig. 4: Schematic of write driver circuit.

The function of the SRAM write driver is to quickly discharge one of the bit lines from the precharge level to below the write margin of the SRAM cell. Normally, the write driver is enabled by the Write Enable (WE) signal and drives the bit line using full-swing discharge from the precharge level to ground. The order in which the word line is enabled and the write drivers are activated is not crucial for the correct write operation. Write driver uses two stacked NMOS transistors to form two pass-transistor AND gates using NMOS Q1,Q3 and Q2,Q4 transistors. The sources of NMOS transistors *Q*1 and *Q*2 are grounded. When enabled by write enable, the input data enables, through inverters 1 and 2, one of the transistors *Q*1 or *Q*2 and a strong "0"is applied by discharging *BL* or *BLB* from the precharge level to the ground level.

4.4 Sense Amplifier

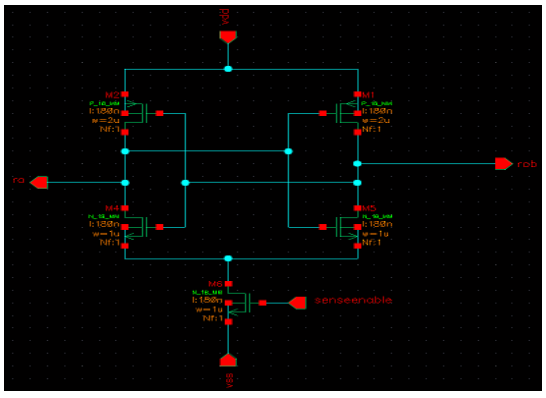

Fig. 4: Schematic of Sense Amplifier.

Sense amplifiers (SA) are an important component in memory design. The choice and design of a SA defines the robustness of bit line sensing, impacting the read speed and power Due to the variety of SAs in semiconductor memories and the impact they have on the final specs of the memory, the sense amplifiers have become separate class of circuits. The primary function of a SA in SRAMs is to amplify a small analog differential voltage developed on the bit lines by a read-accessed cell to the full swing digital output signal thus greatly reducing the time required for a read operation. Since SRAMs do not require data refresh circuitry after sensing, the sensing operation must be nondestructive. Architectures using column multiplexing can share a single SA among the multiplexed columns such that only one column is connected to the sense amplifier at any given time. Generally, the parameters characterizing a sense amplifier include:

• Gain A =Vout/Vin.
• Sensitivity S =Vin min – minimum detectable signal.
• Rise time trise, fall time tfall – 10% to 90% of the signal transient.

A latch-type SA is shown in Figure 5. This type of a SA is formed by a pair of cross-coupled inverters, much like a 6T SRAM cell. The sensing starts with biasing the latch-type SA in the high-gain metastable region by precharging and equalizing its inputs. Since in the latch-type SA the inputs are not isolated from the outputs, isolation transistors are needed to isolate the latch-type SA from the bit lines and prevent the full discharge of the bit line carrying a "0", which costs extra power and delay. Due to the presence of the column MUX/isolation transistors, two precharge/equalize circuits are needed to ensure reliable sensing.

4.5 Row Decoder

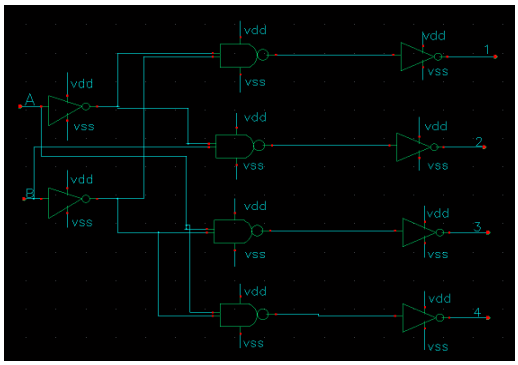

Fig. 5: Schematic of Row decoder.

The above schematic shows a simple and gate based decoder. The function of decoder is to select a particular word line depending on the inputs A and B.The above decoder is 2:4 decoder.

The simple and gate based decoder is used. The 4:16 row decoder has 4 inputs 'A','B', 'C', 'D' and 16 outputs namely '1' to '16'. The outputs of decoder acts as a word line to each row. To illustrate one can consider If A='1', B='0' and C='0' D='0'then the 9th word line is selected. From the above waveform it can be observed that the corresponding word line '9' is selected and it is used for write and read operations.

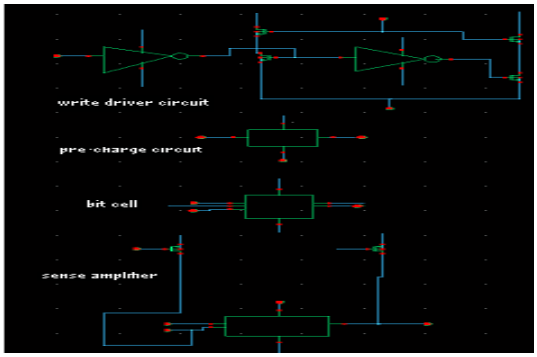

Fig. 6: Schematic of Complete bit cell.

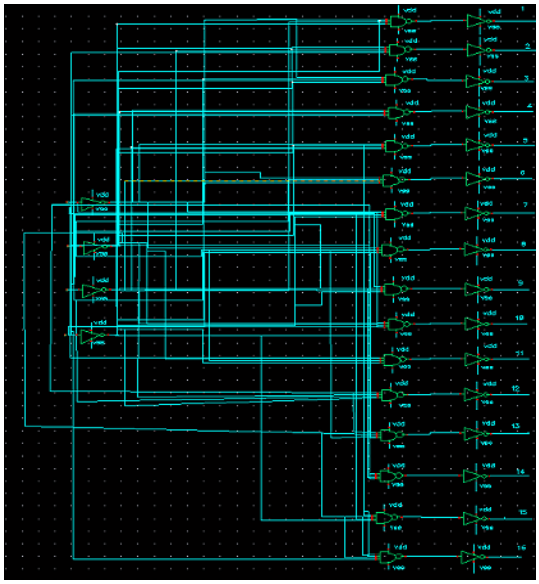

Fig. 7: Schematic of 4:16 decoder.

Table I: Data and Wordline selection.

Input data selection	Wordline Selection
datain	1
datain1	2
datain2	3
datain3	4
datain4	5
datain5	6
datain6	7
datain7	8
datain8	9
datain9	10
datain10	11
datain11	12
datain12	13
datain13	14
datain14	15
datain15	16

The 16x16 memory array is capable of storing 256 bits. It consists of 256 bit cells,16 sense amplifiers,16 pre-charge circuits.16 write driver circuits. As the capacity increases the sizing of the transistors changes due to loading effect. Each column has a single sense amplifier, write driver circuit, pre-charge circuit. The 16X16 memory array has 16 readout signals and readout bar signals. Readout and readout bar signals are complement to each other. The 'A','B','C' &'D' are the row decoder inputs, depending on the particular input combination the corresponding word line and outputs are selected.

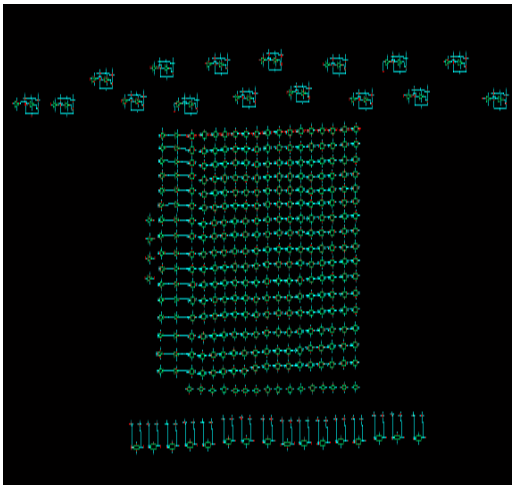

Fig. 7: Schematic of 16X16 memory array.

5. Experimental Results

This Section clearly disscuss about the simulation results of 1x1 memory array,4:16 decoder, 16x16 memory array, the work is carried out on cadence virtuoso the simulation is done using spectre.Fig.8., discuss about transient response for 1x1 memory array forreadandwriteoperations.

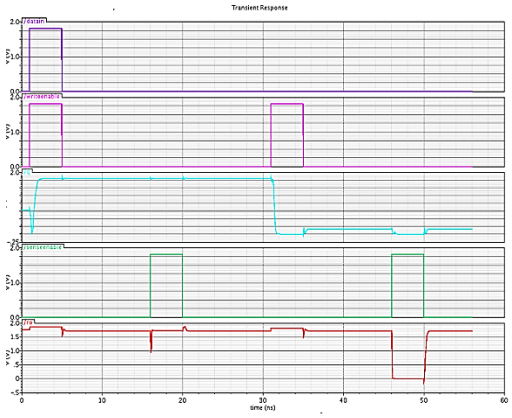

Fig. 8: Transient response for 1x1 memory array.

The figure shows write and read waveforms of 1x1 memory array. The stop time of transient response is 56ns. The duration of writeenable and senseenable signal is set to 4ns. The datain is the input data signal. The writeenable is the write operation control signal. The senseenable is the read operation control signal. Before operation takes place the q output signal is precharged to vdd/2.The write operation can be explained as , when the writeenable

signal goes high to logic '1', the 'q' output goes high hence logic '1' is written into the memory. One can say that logic '1' is stored into the memory. The 'q' output signal retains its earlier value until next arrival of logic '1' write enable signal. The logic '0' is written into the memory i.e. the q output signal goes low logic '0' when second time write enable goes high. The read operation can be explained as , when the senseenable signal goes high to logic '1', the 'ro' output goes high hence logic '1' is read into the memory. One can say that logic '1' is read into the memory. The 'ro' readout output signal retains its earlier value until next arrival of logic '1' senseenable signal. The logic '0' is read into the memory i.e. the 'ro' output signal goes low logic '0' when second time senseenable goes high. Hence write and read operations are explained

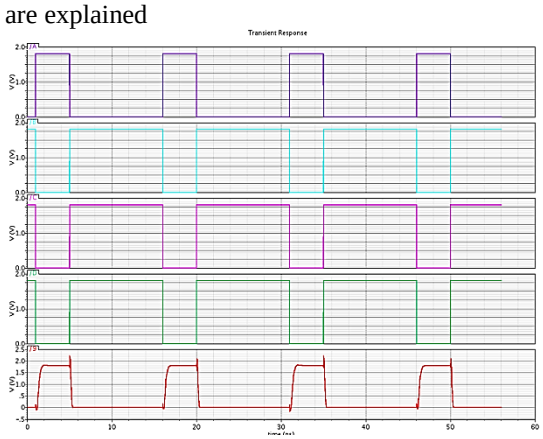

Fig.9: Transient response for 4:16 decoder.

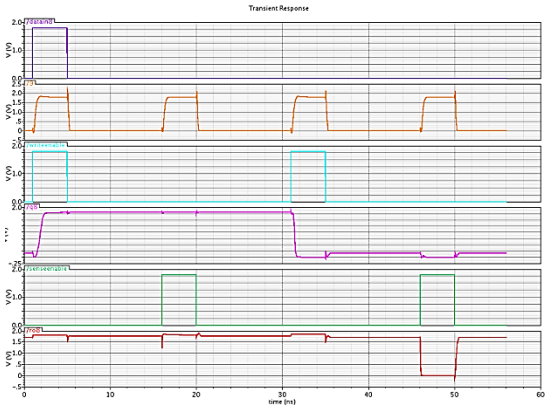

Fig 10: Transient response for 16x16 memory array.

The 16x16 memory array is capable of storing 256 bits. The datain8 is the input data signal. The corresponding wordline'9' is selected which act as a control signal for write and read operation. The corresponding output signals'q8' and' ro8' are write and read signals. The read and write operations are illustrated in the above figure. The write operation can be explained as , when the writeenable signal goes high to logic '1', the 'q8' output goes high hence logic '1' is written into the memory. One can say that logic '1' is stored into the memory. The 'q8' output signal retains its earlier value until next arrival of logic '1' write enable signal. The logic '0' is written into the memory i.e. the 'q8' output signal goes low logic '0' when second time write enable goes high. The read operation can be explained as , when the senseenable signal goes high to logic '1', the 'ro8' output goes high hence logic '1' is read into the memory. One can say that logic '1' is read into the memory. The 'ro8' readout output signal retains its earlier value until next arrival of logic '1' senseenable signal. The logic '0' is read into the memory i.e. the 'ro8' output signal goes low logic '0' when second time senseenable goes high. Hence write and read operations are explained.

.

Conclusion

The schematic is designed for storage capacity of 256 bits i.e. 16x16 Memory array. The complete array which includes pheripheral components such as memory bit cell, write driver circuit, pre-charge circuit, Sense amplifier are designed and integrated. The integrated SRAM Memory is capable of storing 256bits. The proposed work is operated with analog input voltage of 0 to 1.8v, supply voltage 1.8v, and consumes 49.94mW power. The access time is 1.05ns,368ps,175ps,2.65ps for write logic '1' &'0', read logic'1' &'0' respectively. The SRAM is designed and implemented in standard UMC180nm technology of version 5.14 using Cadence virtuoso tool for schematic.

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References

Neil H. E. Weste, David Harris, Ayan Bannerjee (2009), CMOS VLSI Design – A Circuits and Systems Perspective, Pearson Education, 3rd Edition.

Sung-Mo Kang, Yusuf Leblebici (2005) , CMOS Integrated Circuits-Analysis and design, Tata McGraw-hill Edition, 3rd Edition.

Joon-Sung Yang & Gahngsoo Moon (2005) "*32K-BIT SLEEPY SRAM",* Dec.

Andrei Pavlov, Manoj Sachdev (2008), CMOS SRAM Circuit Design and parametric test in nano Scaled technologies-Process-aware SRAM design and test, Springer publications

Jawar Singh, Dhiraj K.Pradhan, Simon Hollis, Saraju P. Mohanty (2008)"A single ended 6T SRAM cell design for ultra low voltage applications" in IEICE 2008, pg 750-755

Neeraj Kr. Shukla, R.K.Singh, and Manisha Pattanaik (2011) " Design and analysis of a Novel Low power SRAM bit-cell structure at Deep-Sub-Micron CMOS technology for mobile multimedia applications" in International Journal of Advanced Computer Science and Applications, pg 43-46 Vol.2, No.5,2011.

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