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Research Article

Protection Mechanism for High Frequency Circuits in Automotive Applications

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Abstract

Electrostatic Discharge (ESD) has become one of the most critical reliability issues in High Frequency (HF) circuits in automotive electronics. Therefore, there have been extensive research efforts seeking to improve ESD protection capabilities; the goal is to achieve highly reliable circuits and products in the presence of ESD threats. However, the continuous scaling of technology and the introduction of new device concepts and materials into the mainstream CMOS technology has brought many new ESD challenges. In this dissertation a variety of ESD issues in advanced CMOS technology are addressed in breadth, covering topics that range from fundamental device physics to circuit design engineering, providing the guidelines needed to develop robust and transparent ESD protection circuits.

Key Words: *Automotive Electronics Design, Circuit Protection, High Frequency Protection*

Introduction

The auto industry's increased use of on-board electronics for guidance, entertainment and safety control systems. It has created substantial integrated circuit and system-on-chip (SoC) based design challenges to deliver energy and cost-efficient – yet highly reliable – electronics systems. As the use of on-board electronics in vehicles rises, power management plays a more critical role in automobile reliability.

To address power management, microcontroller units and other chips controlling on-board systems require a lower voltage and higher frequency rate to ensure consistent, reliable and fast operations. The solution enables design teams to obtain deeper insight into circuit power consumption and reliability measures at an early stage. It also allows implementation of power-optimization techniques, failure models & risks. Providing early analysis, reduction and design optimization assists in meeting the expected requirements and increasing overall electronic circuit efficiency.

High Frequency Circuits in Automotives

Almost half the value of next-generation automobiles is expected to come from onboard electronics and electromechanical components. Manufacturers in this industry are using advanced electronics within sophisticated engine and safety controls and electric/hybrid electric drives as well as in the design of navigation, audio systems and LED lighting. As a result, automotive electronics engineers face a variety of design challenges.

Automobiles and automotive markets represent a growing area of opportunity for suppliers of high-frequency components and hardware. When looking at electronic systems or more specifically ECUs (electronic control units) for these systems, however, growth is expected to be much stronger. Nowadays, electronics run pretty much everything in a vehicle. Between consumer love of electronic conveniences and hybrid or electric vehicles, the use of electronic systems in the automotive industry is accelerating at a furious pace. Of course, with new technologies, comes new challenges. Among the design trends are faster transports; more wireless applications, often using a variety of standards; higher switching power, especially when talking about hybrid or electrical vehicles and the sheer amount and density of electronics in modern vehicles.

ESD Failure

On-board electronic systems can impede each other's operation due to electromagnetic interference (EMI) noise, which can further compromise reliability. Commonly, electrostatic charges are created by the contact and separation of two materials. Once charges are created and remain on a material, they become electrostatic charges. The imbalance of charges produces an electric field

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between material bodies. Meanwhile, the built-up electric field can result in the transfer of charges due to the electrical potential difference. This phenomenon is known as Electro Static Discharge (ESD).

There is no more demanding environment for power CMOSs than automotive systems. As the components controlling the power for on-board electronics, CMOSs in automotive systems are frequently used close to their electrical and thermal absolute maximum ratings in an effort to maximize power-to-weight ratios, i.e. to minimize material usage and minimize the physical volume of circuitry, in addition to cutting costs.

Design engineers have at their disposal sophisticated analysis tools to verify the adequacy of each component. Failure rates are extremely low, on the order of a few per million. The rarity of failure makes it extremely difficult to identify the cause of those failures that do occur. Collaborative efforts from both power CMOS manufacturers and automotive design and manufacturing houses are required to reach successful solutions and in many cases, proving the effectiveness of these solutions is extremely difficult due to the low failure rates involved.

ESD Protection Design for HF Circuits

As the demand for wireless HF and high speed mixed-signal systems is rapidly increasing, on chip ESD protection design for these systems has posed a tremendous challenge. While providing sufficient immunity to the ESD stresses, ESD protection devices should not affect the signal under normal operating conditions. However, the ESD protection devices introduce parasitic capacitances and resistances, and the capacitance associated with the ESD protection devices can be several pF. In the GHz frequency system, the reactance due to this large capacitance becomes comparable to the characteristic impedance at the interfaces (typically 50 Ω), causing reflections of the signals, inefficient power transfer etc. The ESD devices can also generate noise or exacerbate the substrate noise coupling problem.

Because of these negative effects on the circuit performance, there used to be a "sign-off waiver" for the ESD protections of HF Circuits, which means that no ESD protection or only limited size of ESD protection devices were installed at the inputs of HF circuits. However, due to the integration of today's complex mixed-system in CMOS technologies, there is no longer any differentiation between HF pins and digital pins; therefore, there should be no difference in their ESD performance.

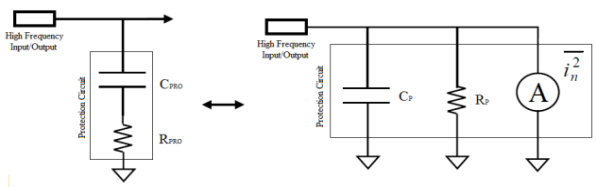

Figure-1: A simplified model of ESD protection circuit and its parallel configuration

As the number of HF pins per device increases, the ESD robustness of the HF pins has become a critical factor in determining the yield ratio. Thus a good methodology to provide sufficient ESD protection capability with tolerable interference to the HF performances is required. To develop a good HF ESD protection scheme, at first the nature of ESD-to-circuit impact should be understood.

HF Modeling of ESD Protection Devices

The compact models of ESD devices can be simplified to a series connection of a capacitor (C_{PRO}) and a resistor (R_{PRO}), as depicted in Fig-1. At a given frequency (ω), this series configuration can be transformed to the parallel configuration in Fig-1. The quality factor (Q) is defined as in Eq.1. Assuming Q >> 1, *Rp* and *Cp* in Fig-1 can be expressed as in Eq.2 and 3.

$$Q = 1 / (\omega R_{PRO} C_{PRO}) \quad (1)$$

$$R_P \approx Q^2 R_{PRO} = Q / (\omega C_{PRO}) = 1 / (\omega^2 R_{PRO} C_{PRO}^2) \quad (2)$$

$$C_P \approx C_{PRO} \quad (3)$$

In Fig-1, a thermal current-noise source ($\overline{i_n^2}$) is also included, and it can be described as follows,

$$\overline{i_n^2} = (4kT\Delta f)/ R_P = 4kT\Delta f\, \omega^2 R_{PRO} C_{PRO}^2 \quad \text{------ 4}$$

The simple RC model in Fig-1 is suitable for most of ESD devices, especially for the diode structures. More sophisticated models may be needed to deal with more complex devices. Fig-2 shows an RF model for a gate-grounded NMOSFET, which has drain-gate capacitance (Cdg), parasitic drain resistance (Rd), gate resistance (Rg), drain-body capacitance (Cdb), and substrate resistance (Rs). However, at a specific frequency level, this complex RC model can also be simplified to one resistance and one capacitance by successive impedance transformations.

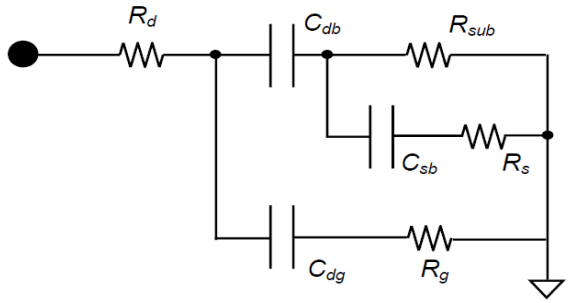

Figure-2: A compact RF model of gate-grounded MOSFETs.

First, we will discuss the impact of Rp and Cp on the HF performance. Depending on the type of on-chip ESD protection devices, C_{PRO} can range from several hundred

fF* to several pF. Recently, approximately 200 fF protection devices with a protection level higher than 2kV HBM have been reported. In general, we can ignore the loading effect of R_{PRO}, because R_{PRO} is usually larger than 1 kΩ. However, the loading effect of parasitic C_{PRO} at the multi-GHz system can significantly alter the input/output matching, degrading the power-transfer-efficiency in HF circuits. C_{PRO} also limits the bandwidth of high speed digital inputs / outputs.

* Femtofarad is a very small unit and therefore it is rarely used in electronics and electrical engineering (1 picofarad [pF] = 1000 femtofarad [fF])

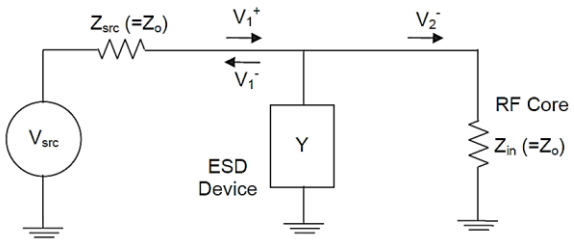

Figure-3: A two-port model of an HF Input/Output with an ESD protection device. (Y represents the ESD protection device)

Fig-3 illustrates a generic example of HF input/output circuits with an ESD protection device. The HF input impedance (Zin) is perfectly matched to the source impedance (Zsrc), e.g. Zo (typically 50 Ω); then ESD protection devices are added between the input source and the matching network. As mentioned before, at high frequencies, C_{PRO} alters the input matching and degrades S11 and S21: S11 is the input refection s-parameter. The ratio of the reflected signal (V_1^-) to the incident signal (V_1^+); S21 is the forward transmission s-parameter, and the ratio of the outgoing signal (V_2^-) to the incident signal (V_1^+). S11 and S21 for the system in Fig-3 can be expressed as follows

$$S11 = V_1^- / V_1^+ = (-Z_O Y) / (2 + Z_O Y) \quad (5)$$

$$S21 = V_2^- / V_1^+ = 2 / (2 + Z_O Y) \quad (6)$$

S11 of the system in Fig-3 is plotted in Fig-4 with the C_{PRO} of 200 fF, S11 is below -10 dB even at a signal frequency of 10 GHz. However a 1 pF C_{PRO} causes a considerable signal reflection; resulting in -10 dB S11 at approximately 2.3 GHz. Fig-5 shows the power loss represented by S21 versus frequency.

With 200 fF C_{PRO}, the power loss is 0.54 dB at 10 GHz. However, if C_{PRO} is larger than 1 pF, the power loss increases to over 5.5 dB. That is, the power loss is extremely sensitive to the size of ESD protection devices at multi-GHz frequencies. This loading effect of C_{PRO} has been fully analyzed, with a single ESD device and multiple distributed devices. It should be pointed out that for the analysis in Figs. 3 to 5; we have not included the capacitance and inductance of the package, which could be larger than pf and nH levels, respectively. However, assuming a certain package type and the relevant parasitic impedance, we can apply a similar approach to estimate the impact of ESD protection devices on input/output impedance matching and bandwidth limit.

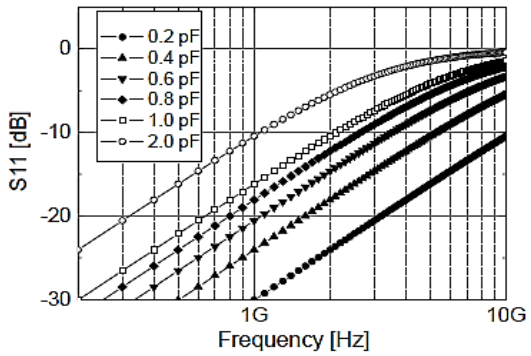

Figure-4: S11 with a variety of CESD

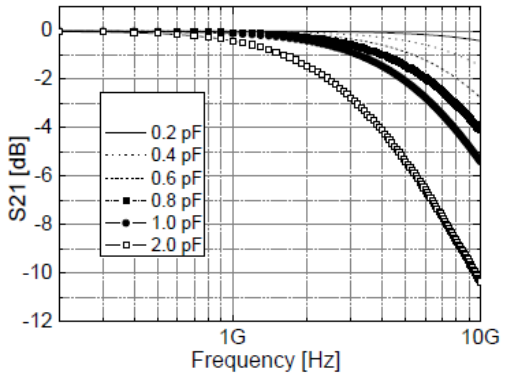

Figure-5: S21 with a variety of CESD

ESD Protection Strategies for HF Circuits

One of the straight forward methods to address the matching alteration problem due to C_{PRO} is minimizing the size of ESD protection devices. This method is often called lower-C ESD design. This lower-C method implies that the ESD device is sized to barely meet the ESD immunity requirements or sacrifice the ESD robustness to guarantee better HF performance. In this approach, it is possible that ESD protection circuits are selected from an ESD library and attached to input / output's perhaps after finishing the HF core circuit design, expecting the ESD protection devices have a negligible impact on the RH performance. Engineering work here is primarily focused on the optimization of the ESD kit to minimize the parasitic capacitance.

The counterpart of the lower-C ESD design is the 'ESD-HF co-design' concept. A simple example of the co-design approach is to consider ESD protection devices to be a part of the matching network, and include a certain ESD protection device at the very beginning of HF circuit design. In many cases, the matching alteration problems can easily be solved using this approach. Some drawbacks of the co-design approach are the high effort required for the HF modeling of ESD protection devices from the early

phase of process development, as well as additional engineering expenses, since ESD developers need to be involved throughout the HF design phase.

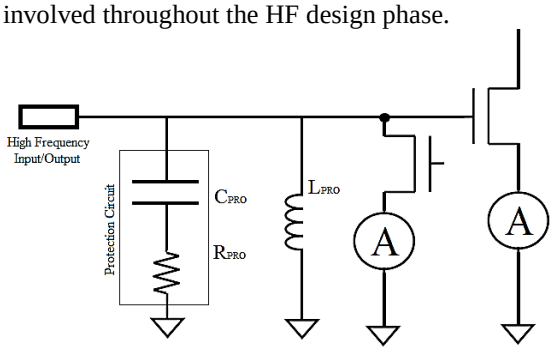

Figure-6: ESD cancellation scheme with an additional inductor

More aggressive examples of 'ESD-HF co-design,' such as 'ESD cancellation' and 'ESD-isolation' have been demonstrated. The 'ESD cancellation' scheme depicted in Fig-6 has an additional on-chip inductor in parallel with the ESD protection devices. At a given HF signal frequency, this inductor resonates out the capacitance of the ESD protection device (C_{PRO}); therefore the ESD protection device is virtually invisible in the normal operations.

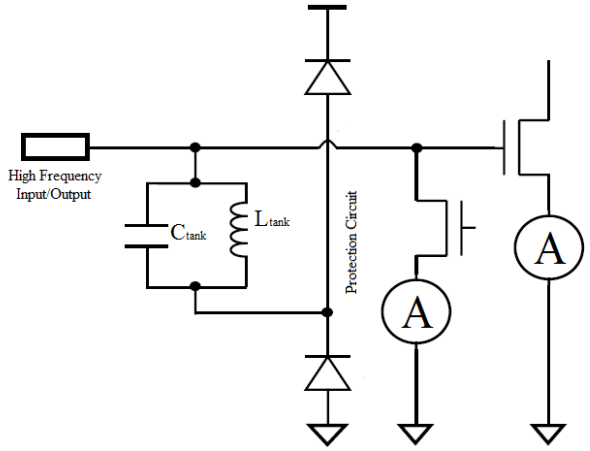

Figure-7: S_{21} ESD Isolation scheme with an LC-tank

The concept of 'ESD-isolation' is similar to 'ESD cancellation'. As illustrated in Fig-7, LC-tank is inserted between the input path and the ESD protection devices. The LC tank should be tuned so that the resonant frequency is matched to the HF signal frequency; which 'hides' the ESD protection devices from the input path at the signal frequency. Unfortunately, the 'ESD cancellation' and 'ESD isolation' schemes have several drawbacks or limitations. For example, in these protection schemes, at least one additional on-chip inductor is needed.

This large on-chip inductor may be considered to be an excessive expense in improving ESD immunity. Furthermore, to minimize the signal loss due to the inductor, the quality factor of the inductor must be high, which is the case only in mature HF processes. A fundamental limitation is that the ESD protection schemes with inductors can be applied only to narrow-band HF circuits, since cancellation or isolation occurs at a certain frequency.

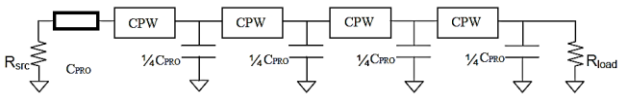

Figure-8: Four-segment distributed ESD protection system.

For broad band applications, several approaches have been proposed during the past few years. Four-segment distributed ESD protection system is shown in Fig-8. The four segments of ESD protection devices and the CPW (coplanar waveguide) compose an artificial transmission line with characteristic impedance, the same as the source and HF input impedance, thereby avoiding the impedance discontinuity due to a large single capacitance of the conventional ESD protection device.

The CPW should be designed to obtain the desired characteristic impedance

$$Z_O = \sqrt{((L_{CPW}) / (C_{PRO} / C_{CPW}))} \quad (7)$$

Where, L_{CPW} and C_{CPW} are the inductance and the capacitance of the CPW. In MOS gate, ground protection devices are employed. It is well known that non-uniform conduction of the grounded gate MOSFET can easily limit the ESD protection effectiveness unless the layout is carefully optimized with respect to symmetry; the ballasting resistors are placed in series with the ESD devices.

The ESD protection structure in Fig-8 is likely to exacerbate this non-uniform conduction issue and a large current is shunted by only the first few segments close to the input/output pad. However in the measurement results with HBM and CDM stresses, demonstrated that each small segment can effectively be turned on, which is probably due to the wide (~36 μm) metal lines between segments and the N-well ballasting resistors in series with the ESD protection devices.

A drawback of this ESD protection scheme is its large size because it needs long CPWs between the segments to achieve a sufficient inductance. The structure recommended is 0.35 mm ~ 1.4 mm length; its application would be limited to the circuits with a few high-speed interfaces.

For high-speed digital applications, the T-coil has been used in part of ESD protection structures as illustrated in Fig-9. With proper choice of *LT*, *CB* and the coupling coefficient between the two inductors with respect to *RT* and the impedance at the node *X*, *ZIN* can be equal to *RT* over wide frequency range.

However, the ESD test results show that HBM stress tolerance is only 800-1000 V although it has a large (1.2

pF) ESD protection device. In this ESD protection scheme, the on-chip inductors are involved in the ESD current path. The series resistance of the T-coils may cause this low ESD immunity, and the abrupt turning at each corner of the T-coil layout could be vulnerable due to electro migration under ESD conditions.

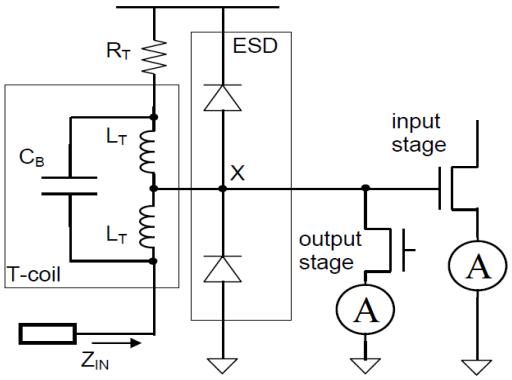

Figure-9: T-coil network for ESD protection

Summary

The impact of ESD parasitic elements on the performance of HF circuits has been analyzed with a simplified HF model of ESD protection devices. The degree of signal reflection and power loss is extremely sensitive to the size of ESD protection devices at multi-GHz frequencies; at 10 GHz, the input reflection S-parameter (S11) becomes approximately -10 dB with 0.2 pF ESD devices. During the past few years, there have been many studies seeking to overcome this ESD-to-circuit impact, including optimization of the conventional ESD protection devices, co-design methods such as ESD cancellation/isolation and several broadband techniques etc. At relatively low frequencies, the lower-C design methods can be well adopted since it is very simple and transparent to various HF designs. For extremely high frequency applications only co-design methodologies can provide the ESD protection capability without substantial degradation of RF performance. For the medium frequency range around 5 GHz, the trade-off between the lower-C protection and rigorous co-design schemes must be considered.

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