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Research Article

Harmonics Mitigation and Switching loss reduction using Cascaded Multilevel Based Half Bridge and Full Bridge Inverter System

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Abstract

Multilevel converters have been introduced as static high-power converters for medium- to high voltage applications such as large electric drives, reactive power compensations, and FACTS devices. The multilevel converters synthesize a desired stepped output voltage waveform by the proper arrangement of the power semiconductor devices from several lower dc voltage sources. The main advantage of multilevel converters is the use of mature medium power semiconductor devices, which operate at reduced voltages. As a result, the switching losses and voltage stress on power electronic devices are reduced. Also, the output voltage has small voltage steps, which results in good power quality, low-harmonic components, and better electromagnetic compatibility. Multilevel converters have obtained more and more attention in recent years and new topologies with a wide variety of control strategies have been developed. Among the multilevel Converters, the cascaded H-bridge topology (CHB) is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels.This paper gives the MATLAB/SIMULINK analysis of three-phase, five-level and seven level cascaded multilevel voltage source inverter based DSTATCOM and active power filter with various PWM techniques for power line conditioning to improve power quality in the power distribution network.

Keywords: *PWM technique, Cascaded multilevel voltage source inverter, Cascaded H- Bridge topology , Harmonics, Power quality.*

1. Introduction

The power quality problems include high reactive power burden, harmonic currents, load unbalance, excessive neutral current etc. Electrical Power Quality had obtained more attention in power engineering in recent years. Multilevel converters have obtained more and more attention in recent years and new topologies with a wide variety of control strategies have been developed for the improvement in the power quality. There are three different basic multilevel converter topologies: neutral point clamped (NPC) or diode clamped, flying capacitor (FC) or capacitor clamped, and cascaded H-bridge (CHB). The main drawback of the NPC topology is unequal voltage sharing between the series connected capacitors, which leads to dc-link capacitor unbalancing and requires a great number of clamping diodes for a high number of voltage levels. Also, the maximum voltage across the switches is closest to the switching node. Therefore, the three-level NPC converter has been commercialized in industry as a standard topology. The flying capacitor multilevel converter and its derivative, the stacked multilevel (SM) converter and use flying capacitors as clamping devices. These topologies have several attractive properties compared to NPC converters, including the advantage of transformer less operation and have redundant phase leg states that allow the switching stresses to be equally distributed among semiconductor switches. But, these converters require an excessive number of storage capacitors for a high number of voltage steps. A double FC multi cell converter has been presented in. This topology has been implemented by adding two low-frequency switches to the conventional configuration of the FC multilevel converter. The main advantages of the presented converter, in comparison with the FC multilevel and SM converters, are the doubling of the rms value of the output voltage and the number of output voltage steps and the canceling of the midpoint of the dc source. But two additional switches must operate at the peak of the output voltage. This restricts high-voltage applications of this converter.

The CHB topology is a good solution for high-voltage applications due to the modularity and the simplicity of control. But, in these topologies, a large number of separated Voltage sources are required to supply each conversion cell. To reduce the number of separate dc

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voltage sources for high-voltage applications, a new configurations have also been presented; however, a capacitor-voltage balancing algorithm is required. Multilevel converters have some particular disadvantages. They need a large number of power semiconductor switches, which increase the cost and control complexity and tend to reduce the overall reliability and efficiency. Although low-voltage rated switches can be utilized in a multilevel converter, each switch requires a related gate driver and protection circuit. This may cause the overall system to be more expensive and complex. The new technologies have strived in to introduce a new multilevel converters circuit with a reduced number of components compared to conventional multilevel converters. This topology consists of series connected sub multilevel converter blocks. In order to create the output voltage with a constant number of steps, there are different structures with different number of components. Therefore, the converter structure can be optimized for various objectives. This increases the design flexibility. But, the converter needs a large numbers of bidirectional switches and the blocking voltage of bidirectional switches is also high. To overcome aforementioned disadvantages, a new topology with reduced number of switches and dc voltage sources has been presented in. Also, the structures based on similar concepts have been presented in.

In these topologies, the dc source is formed by connecting a number of half-bridge sub modules. The main drawback of these topologies is the utilization of unidirectional switches, which operates at high output voltage in single-phase applications. Also, the design flexibility is lost in these topologies. As mentioned the presented topologies, the utilization of switches, which operates at the peak of the output voltage. Therefore, a bulky and costly interface transformer needs to be used for high-voltage applications. This paper proposes a new modular and simple topology for cascaded multilevel converters that produces a large number of steps with a low number of power switches and components.

The multilevel power conversion has been receiving increasing attention in the past few years for high power applications. Numerous topologies have been introduced and studied extensively for utility and drive applications in the recent literature. These converters are suitable in high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltage with a limited maximum device rating. There are various current control methods for two-level converters. Hysteresis control of power converters based on instantaneous current errors is widely used for the compensation of the distribution system as it has good dynamic characteristics and robustness against parameter variations and load non-linearities.

2. Multilevel inverter structures

Multilevel converters share the advantages of multilevel voltage source inverters, they may be suitable for specific application due to their structures and drawbacks. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why most of the time it is referred to as a converter instead of an inverter. A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints, complexity of the controller and of course, capital and maintenance costs.

Three different major multilevel converter structures have been applied in industrial applications: diode clamped multilevel inverter, cascaded H-bridge converter with separate dc sources and flying capacitors. Fig1 shows a schematic diagram of one phase leg of inverters with different number of levels for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor, while the three-level inverter generates three voltages and so on.

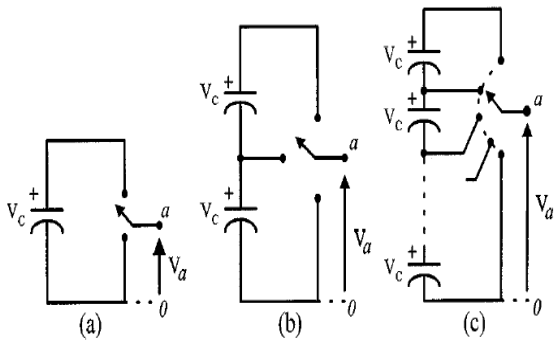


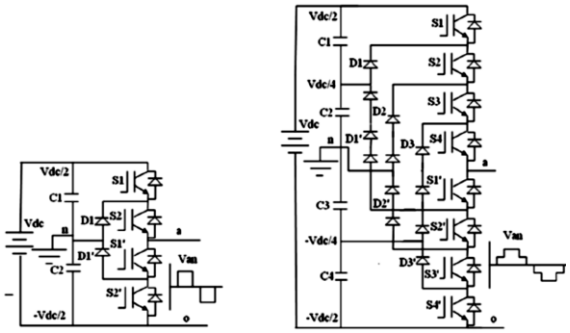
Fig1: One phase leg of an inverter with (a) two levels (b) three levels and (c) n Levels

2.1.DIODE-CLAMPED MULTILEVEL INVERTER

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. . A three-level diode clamped inverter consists of two pairs of switches and two diodes. Each switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. In a three-level inverter each of the three phases of the inverter shares a common dc bus, which has been subdivided by two capacitors into three levels. The DC bus voltage is split into three voltage levels by using two series connections of DC capacitors, C1 and C2. The voltage stress across each switching device is limited to Vdc through the clamping diodes Dc1 and Dc2. It is assumed that the total dc link voltage is Vdc and mid point is regulated at half of the dc link voltage, the voltage across each capacitor is Vdc/2 (Vc1=Vc2=Vdc/2). In a three level diode clamped inverter, there are three different possible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. For a three-level inverter, a set of two switches is on at any given time and in a five-level

inverter, a set of four switches is on at any given time and so on

Fig 2 shows the circuit for a diode clamped inverter for a three-level and a five-level inverter. Switching states of the three level inverter are summarized in table 1.



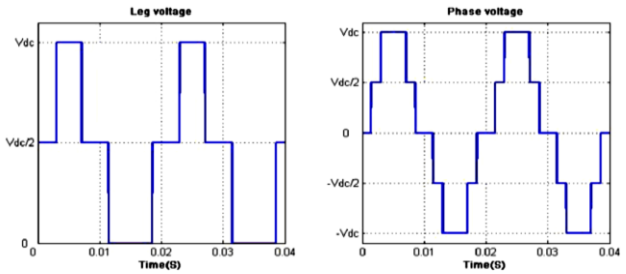
(a) (b)

Fig 2: Topology of the diode-clamped inverter (a) three level inverter and (b) Five –level Inverter

Table 1: Switching states in one leg of the three-level diode clamped inverter

Switch Status	State	Pole Voltage
S_1=ON,S_2=ON S_1=OFF,S_2=OFF	S=+ve	V_{ao}=Vdc/2
S_1=OFF,S_2=ON S_1=ON,S_2=OFF	S=0	V_{ao}=0
S_1=OFF,S_2=OFF S_1=ON,S_2=ON	S=-ve	V_{ao}=-Vdc/2

Fig 3 shows the phase voltage and line voltage of the three-level inverter in the balanced condition. The line voltage V_{ab} consists of a phase-leg *a* voltage and a phase-leg *b* voltage. The resulting line voltage is a 5-level staircase waveform for three-level inverter and 9-level staircase waveform for a five-level inverter. This means that an N-level diode-clamped inverter has an N-level output phase voltage and a (2N-1)-level.



(a) **(b)**

Fig 3: Output voltage in three-level diode- clamped inverter (a) leg voltage and (b) output phase voltage.

In general for an N level diode clamped inverter, for each leg 2(N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. However, capacitor voltage balancing will be the critical issue in high level inverters. When N is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge. Though the structure is more complicated than the two-level inverter, the operation is straightforward.

2.1.1.Operation of DCMLI

Fig 2 shows a three-level diode-clamped converter in which the dc bus consists of two capacitors, C1, C2. For dc-bus voltage Vdc, the voltage across each capacitor is Vdc/2 and each device voltage stress will be limited to one capacitor voltage level Vdc/2 through clamping diodes. To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are three switch combinations to synthesize three-level voltages across a and n.

1. Voltage level Van= Vdc/2, turn on the switches S1andS2.
2. Voltage level Van= 0, turn on the switches S2 and S1′.
3. Voltage level Van= - Vdc/2 turn on the switches S1′, S2′.

Fig 2 shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C1, C2, C3, and C4. For dc-bus voltage Vdc, the voltage across each capacitor is Vdc/4 and each device voltage stress will be limited to one capacitor voltage level Vdc/4 through clamping diodes. Switching states of the five levels inverter are summarized in table 2.

Table2: Switching states in one leg of the five-level diode clamped Inverter

Voltage Vao	Switch state							
	S1	S2	S3	S4	S1'	S2'	S3'	S4'
Vao=Vdc	1	1	1	1	0	0	0	0
Vao=Vdc/2	0	1	1	1	1	0	0	0
Vao=0	0	0	1	1	1	1	0	0
Vao=-Vdc/2	0	0	0	1	1	1	1	0
Vao=-Vdc	0	0	0	0	1	1	1	1

2.2.Flying capacitor structure

The capacitor clamped inverter alternatively known as flying capacitor. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of

using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Fig4 shows the three-level and five-level capacitor clamped inverters respectively.

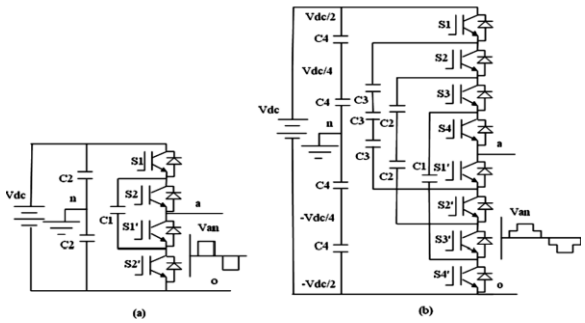


Fig4: Capacitor-clamped multilevel inverter circuit topologies,(a) 3-level inverter (b) 5- level inverter.

2.2.1. Operation of FCMLI

In the operation of flying capacitor multi-level inverter, each phase node (a, b, or c) can be connected to any node in the capacitor bank (V3, V2, V1). Connection of the a-phase to positive node V3 occurs when S1 and S2 are turned on and to the neutral point voltage when S2 and S1′ are turned on. The negative node V1 is connected when S1′ and S2′are turned on. The clamped capacitor C1 is charged when S1 and S1′ are turned on and is discharged when S2 and S2′ are turned on. The charge of the capacitor can be balanced by proper selection of the zero states. In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states, which make up the level V3. Considering the direction of the a-phase flying capacitor current Ia for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. As with the three-level flying capacitor inverter, the highest and lowest switching states do not change the charge of the capacitors. The two intermediate voltage levels contain enough redundant states so that both capacitors can be regulated to their ideal voltages.

Similar to the diode clamped inverter, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an N level converter will require a total of (N-1) * (N-2) / 2 clamping capacitors per phase in addition to the (N-1) main dc bus capacitors.

Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels. The voltage of the five-level phase-leg output with respect to the neutral point n (i.e. Van), can be synthesized by the following switch combinations.

1. Voltage level Van= Vdc/2, turn on all upper switches S1 - S4.
2. Voltage level Van= Vdc/4, there are three combinations.
3. Voltage level Van= -Vdc/4, turn on upper switch S1 and lower switches S1′, S2′and S3′.

2.3. CASCADED Multilevel Inverter

The single phase structures of Cascaded inverter for 3-level, 5-level and 7-level are as shown in fig5

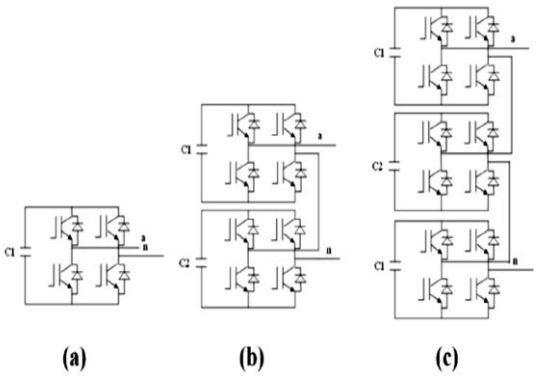


Fig 5: Single phase structures of Cascaded inverter (a) 3-level, (b) 5-level, (c) 7-level

One more alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge inverter. With its modularity and flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers. The CMI synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. By adding more H-bridge converters, the amount of V_{ar} can simply increase without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized. A series of single-phase full bridges makes up a phase for the inverter. A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing. This feature is impossible in other VSC topologies utilizing a common DC link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge converter is provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. Phase-shifted transformers can supply the cells in medium-voltage

systems in order to provide high power quality at the utility connection.

2.3.1. Operation of CMLI

The converter topology is based on the series connection of single-phase inverters with separate dc sources. Fig5 shows the power circuit for one phase leg of a three-level , five-level and seven-level cascaded inverter. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vdc, 0, -Vdc (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from -Vdc to +Vdc with three levels, -2Vdc to +2Vdc with five-level and -3Vdc to +3Vdc with seven-level inverter. The staircase waveform is nearly sinusoidal, even without filtering.

For a three-phase system, the output voltage of the three cascaded converters can be connected in either wye (Y) or delta (Δ) configurations. For example, a wye-configured 7-level converter using a CMC with separated capacitors is illustrated in the fig6.

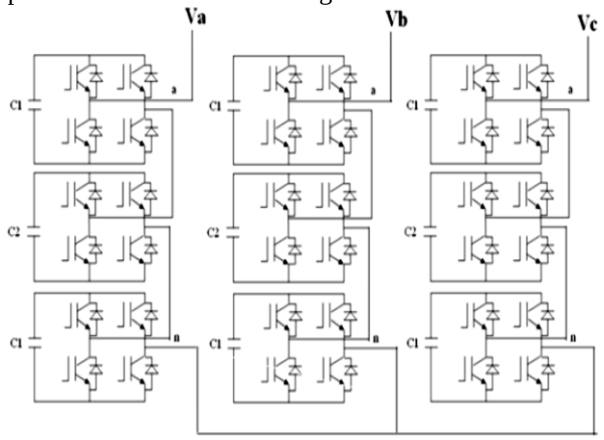


Fig6: Three-phase 7-level cascaded multilevel inverter (Y-configuration)

3. Proposed topologies

3.1 .Introduction

Industrial applications have begun to require higher power rating apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources and drive applications.With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. Among the multilevel Converters, the cascaded H-bridge topology (CHB) is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels.

These converter topologies can generate high-quality voltage waveforms with power semiconductor switches operating at a frequency near the fundamental. Although, in low-power applications, the switching frequency of the power switches is not restricted, a low switching frequency can increase the efficiency of the converter. Additionally, multilevel converters feature several dc links, making possible the independent voltage controls. Additionally, due to its modular structure, the hardware implementation is rather simple and the maintenance operation is easier than alternative multilevel converters. The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources, the so called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems voltage clamping requirement, circuit layout, and packaging constraints. An alternative three-phase cascaded multilevel inverter topology is proposed in this paper. It uses power cells connected in cascade using two inverter legs in series, instead of two parallel inverter legs, as conventionally found in CHB power cells.

3.1.1. CASCADED full bridge inverter

The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. A single-phase two-cell series configuration of such an inverter is shown in Fig7.

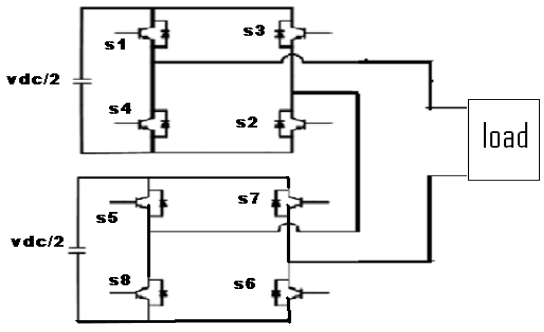


Fig7: Single Phase Structure of 5 Levels H –Bridge Inverter

Each SDCS is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S_1-S_4, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Note that the number of output phase voltage levels is defined in different way from those of two previous inverters. In this topology, the number of output phase voltage levels is defined by m=2s+1, where s is the number of dc sources. Table 3 shows the switch combination of the voltage levels and their corresponding switch states.

Table3: Switching States of single Phase 5 Level Cascaded H-bridge Inverter

Switches ON	Voltage level
S1, S2, S5 and D7	Vdc/2
S1, S2, S6and S5	Vdc
S1, S2, S6 and D3	Vdc/2
S1, D3, S6 and D8	0
S3, S4, S6 and D3	-Vdc/2
S3, S4, S7 and S3	-Vdc
S3, S4, D6 and S3	-Vdc/2
S1, S3, D6 and S3	0

3.2.Cascaded H-Bridge converter

3.2.1. Half H-Bridge

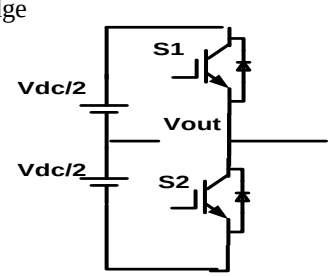


Fig 8: Half Bridge

Fig8 shows the Half H-Bridge Configuration. By using single Half H-Bridge we can get 2 voltage levels. The switching table is given in Table 4

Table4: Switching table for Half Bridge

Switches Turn ON	Voltage Level
S2	Vdc/2
S1	-Vdc/2

3.2.2.Full H-Bridge

Fig 9 shows the Full H-Bridge Configuration. By using single H-Bridge we can get 2 voltage levels. The number output voltage levels of cascaded Full H-Bridge are

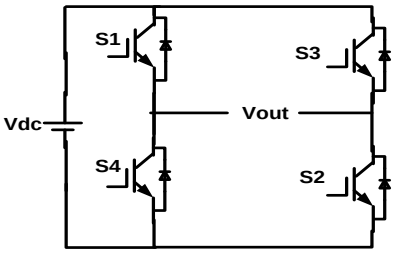


Fig 9: Full H-Bridges

Given by 2n+1 and voltage step of each level is given by Vdc/n. Where n is number of H-bridges connected in cascaded the switching table is given in Table5.

Table5: Switching table for Full Bridge

Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

3.3.Phase multilevel inverter proposed

An alternative three-phase cascaded multilevel inverter topology is proposed in this paper. It uses power cells connected in cascade using two inverter legs in series, instead of two parallel inverter legs, as conventionally found in CHB power cells. The proposed three-phase multilevel inverter is shown in Fig10.This inverter is composed of $(3nL - 3)$ switches and $(3nL - 3)/2$ isolated dc voltage sources, where nL is the number of voltage levels of the line-to-line output voltage. The load can be connected in delta or wye..

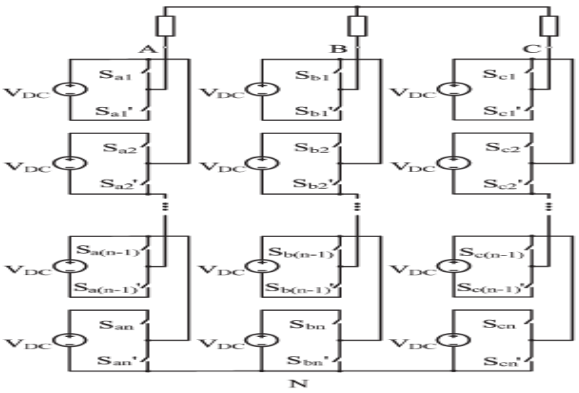


Fig10: Multilevel Inverter Proposed.

The maximum numbers of voltage levels of the line-to-line output voltage vAB(t) and phase-to-neutral voltage vAN(t) are respectively represented by

$nL = 4Nc + 1$ (1)

$nP = 2Nc + 1$ (2)

Where *Nc* is the number of power cells per phase. By construction, the number of voltage levels for this topology is always odd. To understand how each inverter leg should be connected, a detailed analysis of the output voltage of the inverter leg is necessary.

A basic inverter leg with two switches, working in a complementary way, is shown in Fig11(a). Each power cell is composed of two inverter legs with the connections defined in Fig11(b).

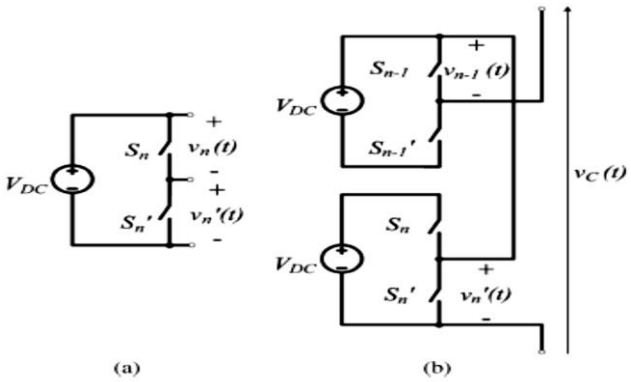


Fig11 (a) Inverter leg connected to the isolated dc voltage source. (b) Power cell using two inverter legs in series.

Table6 shows the switch combination of the voltage levels and their corresponding switch states.

Table 6: Switching States in one Leg of the Five-Level Proposed Cascaded Inverter

Switches ON	Voltage level
Sa1, Sa2′, Sa(n-1) and San′	0
Sa1, Sa2, Sa(n-1) and San′	Vdc/2
Sa1, Sa2, Sa(n-1) and San′	Vdc
Sa1′, Sa2′, Sa(n-1) and San′	-Vdc/2
Sa1′, Sa2′, Sa(n-1)′ and San′	-Vdc

4. Modulation Technique for Multilevel Inverter

Mainly the power electronic converters are operated in the switched mode. Which means the switches within the converter are always in either one of the two states - turned off (no current flows), or turned on (saturated with only a small voltage drop across the switch). Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states (i.e. on and off). This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal. The switched component is attenuated and the desired DC or low frequency AC component is retained. This process is called Pulse Width Modulation (PWM), since the desired average value is controlled by modulating the width of the pulses.For maximum attenuation of the switching component, the switch frequency fc should be high- many times the frequency of the desired fundamental AC component f1 seen at the input or output terminals. In large converters, this is in conflict with an upper limit placed on switch frequency by switching losses. For GTO converters, the ratio of switch frequency to fundamental frequency fc/f1 (= N, the pulse number) may be as low as unity, which is known as square wave switching. These low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. The low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. In these circumstances, multi-level converters can reduce the distortion substantially, by staggering the switching instants of the multiple switches and increasing the apparent pulse number of the overall converter.

4.1. PWM Technique

The fundamental methods of pulse-width modulation (PWM) are divided into the traditional voltage-source and current-regulated methods. Voltage-source methods more easily lend themselves to digital signal processor (DSP) or programmable logic device (PLD) implementation. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level. In discrete current-regulated methods the harmonic performance is not as good as that of voltage-source methods. A sample PWM method is described below.

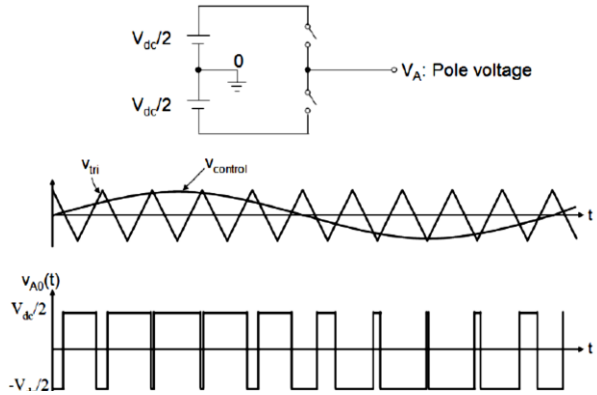


Fig12: Pulse-width modulation

Inverter output voltage, VA0 = Vdc/2, When $V_{control} > V_{tri}$, and VA0 = -Vdc/2, When $V_{control} < V_{tri}$.

PWM frequency is the same as the frequency of V_{tri}. Amplitude is controlled by the peak value of $V_{control}$ and

Fundamental frequency is controlled by the frequency of $V_{control}$.
Modulation Index (m) is given by:

$$m=\frac{v_{control}}{v_{tri}}=\frac{peak\ of\ (V_{AO})_1}{V_{dc}/_2},$$

Where (VA0)1 is the fundamental frequency component of VA0

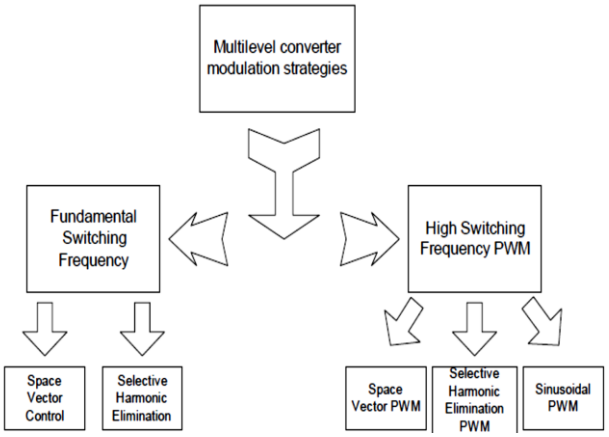


Fig13: Classification of PWM multilevel converter modulation strategies

Voltage-source modulation has taken two major paths; sinusoidal modulation in the time domain and space vector modulation in the q-d stationary reference frame. Sinusoidal and space vector modulation are exactly equivalent in every way. Adjusting some parameters in the sine-triangle scheme (such as the triangle shape and sine wave harmonics) is equivalent to adjusting other parameters in the space vector scheme (such as the switching sequence and dwell time).

5. Comparison between the Proposed Inverter And CHB Multilevel Inverter

Many Characteristics of the proposed topology have been described in this paper. The main difference between the proposed topology and a CHB inverter is the way how the inverter legs are connected. These two converters have the same number of switches on each power cell; thereby, the voltage levels generated in the terminals of each power cell are the same. Thus, the numbers of voltage levels of the phase-to-neutral voltage (V_{AN}) and line to- line output voltage (V_{AB}) will also be the same, as described in Table7.Each power cell in the proposed topology employs double the number of isolated dc voltage sources, with half the power.

The PWM phase-shifted multicarrier modulation technique used in the proposed topology is similar to that used in CHB multilevel inverters. However, if other modulation techniques are employed, for instance, PWM level-shifted multicarrier modulation or space vector modulation, accurate analysis should be done.

Table7: Comparison between Proposed Inverter and CHB Inverter

Topology	Proposed inverter	Cascaded H-bridge inverter
Phase-to-neutral voltage levels	np	np
Line-to-Line Voltage Levels	3np-1	3np-1
Number of power cells per phase	(np-1)/2	(np-1)/2
Number of switches per phase	2(np-1)	2(np-1)
Number of isolated dc voltage sources per phase	(np-1)	(np-1)/2
Load voltage THD	similar	similar
Modulation strategy	similar	similar
Power of each isolated dc voltage source	(Pnominal)/3(np-1)l	(Pnominal)/3(np-1)l

THDs in the load current and line-to-line output voltage were compared in those two converters with the same parameters. Similar results are obtained by using numerical simulations (PSIM software). Harmonic spectrum for the proposed topology was defined and an equivalent illustration for CHB multilevel inverters using PWM phase-shifted multicarrier modulation can be found in showing the similarity between them.

6. Simulation and results

6.1. Simulation of single phase cascaded full bridge inverter for 5 level

A single-phase structure of a5-level cascaded inverter is illustrated in Fig14. Each separate dc source is connected to a single-phase full-bridge or H-bridge inverter. Each inverter level can generate five different voltage outputs, $+V_{dc}$, 0, Vdc/2, -Vdc/2 and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. full bridge Multilevel Inverter

Five level inverter is modeled based on the theoretical concepts. Here the sub system for pulse generator is modeled where one reference wave (sine wave) and four carrier waves (triangular wave) are taken. Here we are taking four carrier signals. Two of them are applied across the positive half cycle of the modulating signal, remaining two of them are applied across the negative half cycle of the modulating signal. From these signals eight PWM signals are generated and then given to the eight switches of a leg. Similarly the pulses are generated for remaining phases.

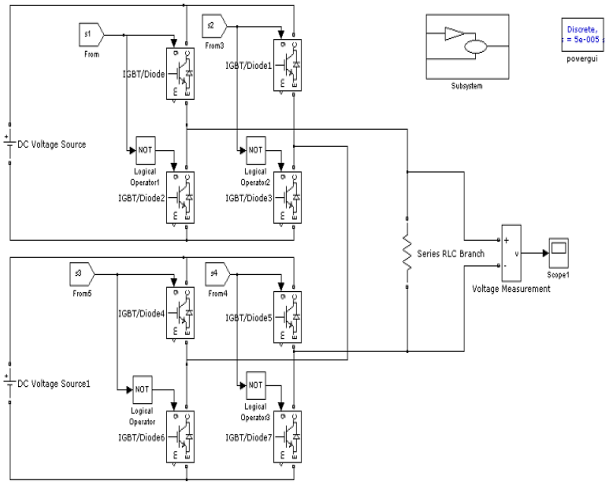


Fig14: Matlab/Simulink model of five –level Cascaded

Based on the concepts explained in modulation techniques, four pulses are generated. Theses pulses are given to the switches in one phase leg of a five level inverter. Similarly the pulses are generated for remaining two phases, just by changing phase shifting angle of modulating signal by 90 degrees. Fig15 represents the carrier modulation signals of the 5-level inverter where one sinusoidal wave is compared with four triangular waves.

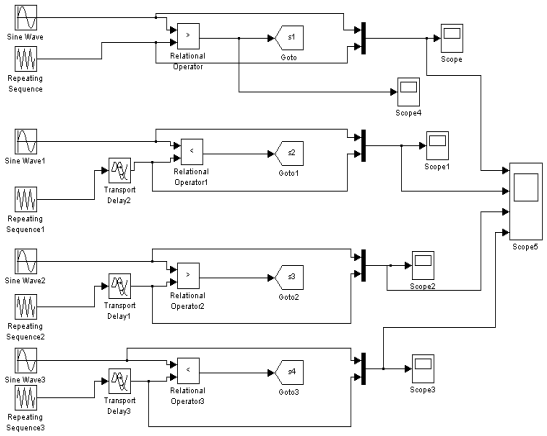


Fig15: Modulation Strategy for five –level Cascaded full bridge Multilevel Inverter

6.1.1. Simulation results

Fig16: show the phase voltage, of a 5-level inverter. Each inverter level can generate five different voltage outputs, $+V_{dc}$, 0, Vdc/2, -Vdc/2 and $-V_{dc}$.

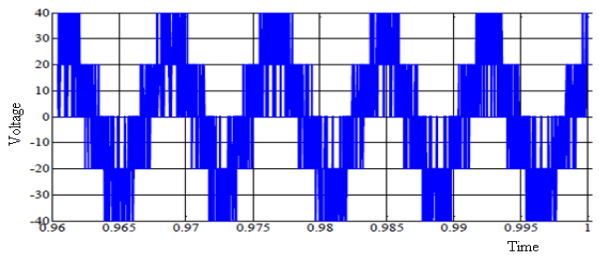


Fig16: Five level output of phase voltage.

6.2. Simulation of three phases cascaded multilevel inverter

A three-phase multilevel inverter was implemented using an inductive–resistive load (displacement power factor of 0.93), connected in delta, with a modulation index of 0.8 and a carrier wave frequency of 1260 Hz. The converter is supplied by the power grid (220 V and 60 Hz). The frequency modulation index is defined by

$$m_f=\frac{f_c}{f_o}$$

Where *fc* and *fo* are the frequencies of the modulating and carrier waves respectively. The load voltage will reach maximum voltage due to the nine levels imposed. A 12-pulse rectifier was used in each cell to obtain a better performance. Fig17 shows a multilevel inverter schematic and a picture of the complete circuit implemented.

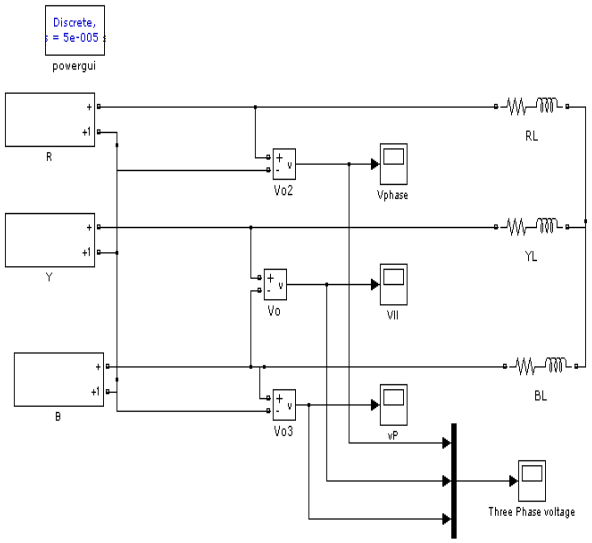


Fig17: Matlab/Simulink model of three phase Cascaded Multilevel Inverter

Fig18(a) and Fig18(b) are arranged in R-Y-B phase's subsystems Depending on the system requirements and the type of the converters employed, the line-side and motor-side filters are optional. A phase-shifting transformer with multiple secondary windings is often used mainly for the reduction of line-current distortion. The rectifier converts the utility supply voltage to a dc voltage with a fixed or adjustable magnitude. The commonly used rectifier topologies include multi pulse diode or thyristor rectifiers and pulse width modulated (PWM) rectifiers. The dc filter can simply be a capacitor that provides a stiff dc voltage in voltage-source drives or an inductor that smoothens the dc current in current source drives.

In the three phase cascaded multilevel inverter, here we are using same modulation strategy as used in above inverter circuit, that is phase shift multicarrier modulation technique is used . All the triangular carriers have the same frequency and the same peak to- peak amplitude and phase shift between two adjacent carrier waves to increase harmonic cancellation. Only the upper switch-gate signals for one phase, because the lower switch-gate signals are

complementary. The other two phases are shifted by + or - 120^0.

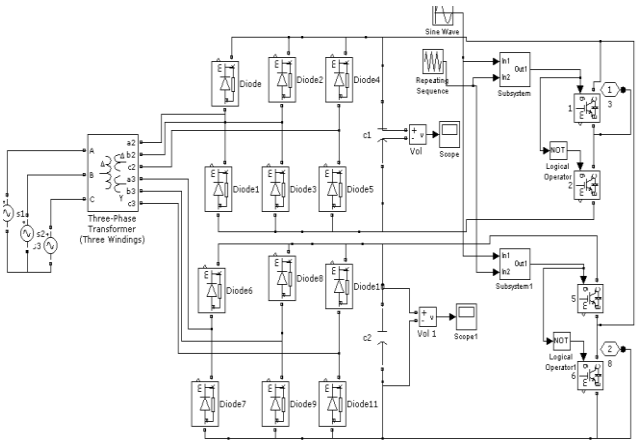


Fig18(a:) Matlab/Simulink model of three phase Cascaded Multilevel Inverter (R-Y-B) phases subsystems

The resultant signal will be high, when the instantaneous value of the sinusoidal wave exceeds the triangular carrier, otherwise, it will be low. The duration of each pulse width in the output comparator depends on the time that the sine wave remains above the value of the triangular wave. These high-frequency pulses are sent to the switches of the circuit with four inverter legs in cascade.

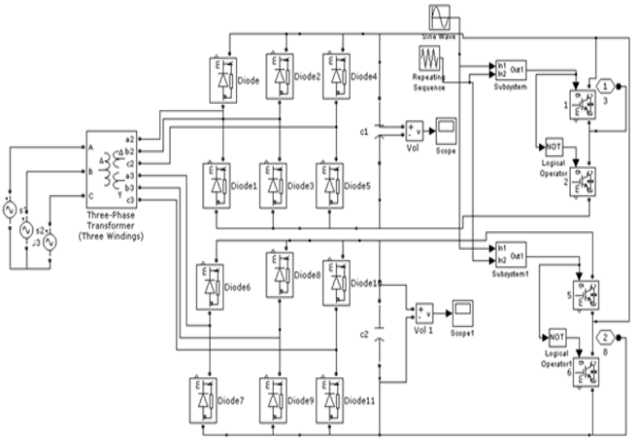


Fig18(b): Matlab/Simulink model of three phases Cascaded Multilevel Inverter (R-Y-B) phases subsystems

The difference here is the number of carrier signals. Here we are taking four carrier signals. Two of them are applied across the positive half cycle of the modulating signal, remaining two of them are applied across the negative half cycle of the modulating signal. From these signals eight PWM signals are generated and then given to the eight switches of a leg. Similarly the pulses are generated for remaining phases.

6.2.1. Simulation results

Figs 19 - 20 show the phase voltage, line voltage and THD of three phase cascaded multilevel inverter. Figures shows the five level output voltage of phase to ground sequences and nine levels output of phase to phase sequences respectively.

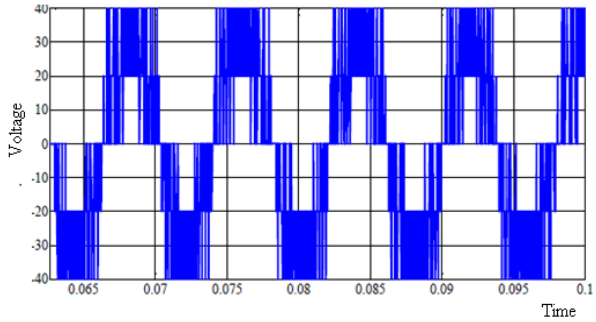


Fig19: Five level output of phase to ground voltage

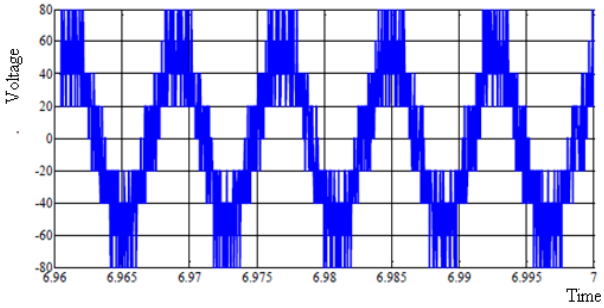


Fig20: Nine level output of Line to Line voltage

6.2.2. Total Harmonic distortion

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

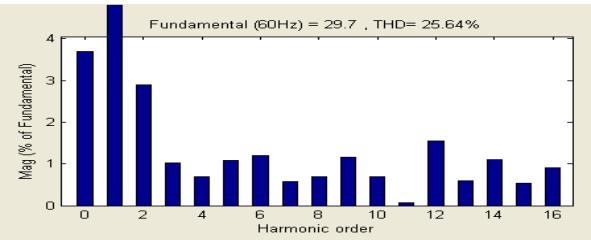


Fig21: Harmonic Spectrum of Phase Voltage

6.3. Simulation of three phase cascaded hybrid h-bridge multilevel inverter system connected to induction motor

Fig22 shows the Mat lab/Simulink model of combination of cascaded half bridge and full bridge multilevel inverter, and input of the inverter is coming by using ac to dc conversion and directly fed to hybrid multilevel inverter. Fig22 shows the topology of the proposed a 7-level 3-phase cascaded hybrid multilevel inverter. Single phase topology of the hybrid multilevel inverter is shown in Fig22(a); the bottom is one leg of a standard 3-leg inverter with a dc power source (Vdc), the top is a hybrid in series

with each standard inverter leg that the H-bridge inverter can use a separate dc power source (Vdc/2).

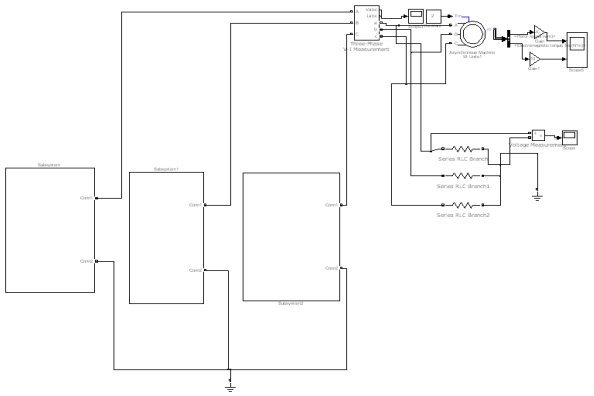


Fig22(a): Matlab/Simulink model of three phase cascaded half and Full bridges MLI system with IM.

When switching operation of this hybrid multilevel inverter topology is switches (s1,s6,s4,s7)is ON the output voltage is zero, switch(s2,s6,s4,s7) is ON the output voltage is Vdc/3, switches (s1,s3,s4,s7) is ON the output voltage is 2Vdc/3, and the switches(s2,s3,s4,s7) is ON the output voltage is Vdc.Here we are using 8 switches and in each phase we get seven output voltage levels in phase – ground voltage .The output voltage seven levels are (0, Vdc/3, 2Vdc/3, vdc, -Vdc, -2Vdc/3, -Vdc).In this inverter system a induction motor is connected to find out the speed and torque of the motor.

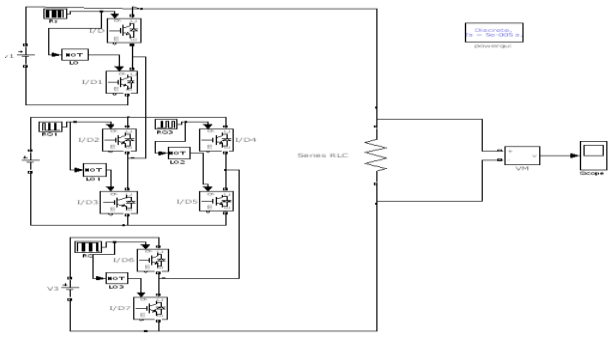


Fig22(b): Matlab/Simulink model of single phase cascaded half and Full bridges multilevel inverter system (R-Y-B phases)

In this topology we are using eight switches as shown in above simulation circuit but we get seven output voltage levels. The THD will be decreased by increasing the number of Levels.

6.3.1.Simulation results

Fig23 shows the phase voltage, motor speed & torque of a seven -level inverter. The speed and torque ripples are very less as compared to another level inverter. Dynamic response is also better for seven level inverter from the observation of speed and torque waveforms.

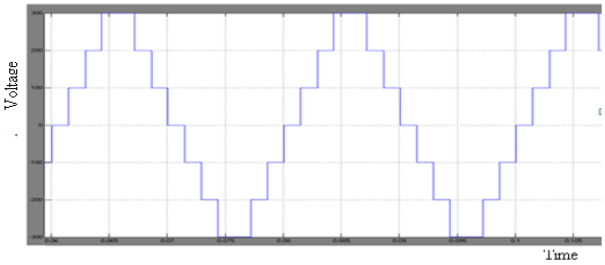


Fig 23: seven level output of phase to ground voltage

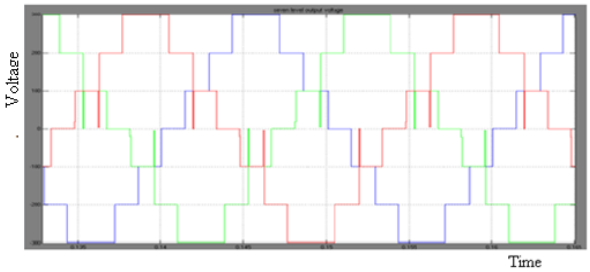


Fig24: Seven level output voltage of three phase hybrid multilevel System for (phase to ground)

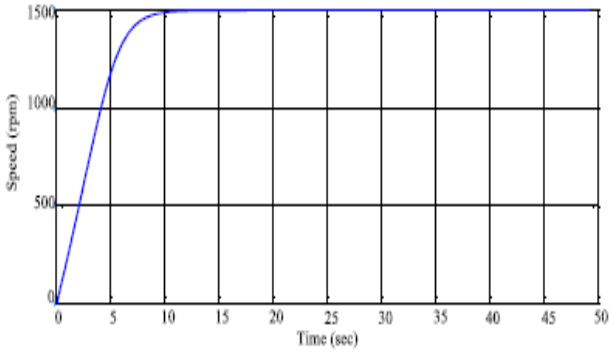


Fig 25: Output waveforms of speed

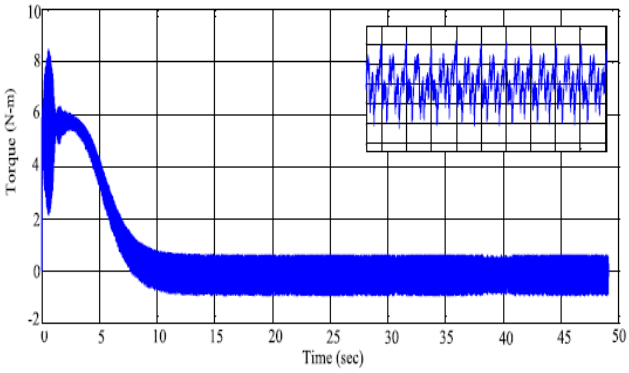


Fig 26: Output waveforms of torque

6.3.2 Total Harmonic distortion

The total harmonic distortion (THD) is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. Here we are using a filter to eliminate the harmonic components. Fig27 - 28 represents the harmonic spectrum analysis of a seven level inverter. In this case the Total Harmonic Distortion is 16.97 % for without filter and 2.57 % for with filter.

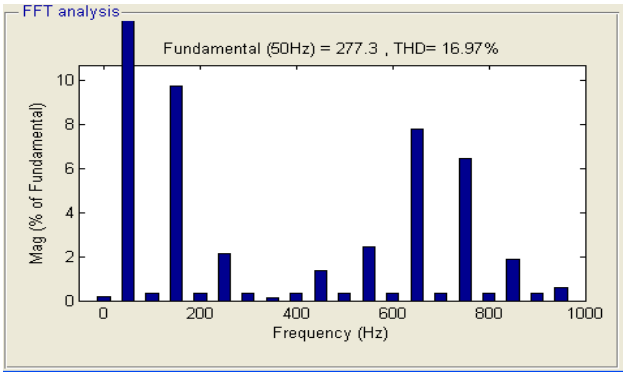


Fig 27: THD of Seven Level Output Voltage without Filter

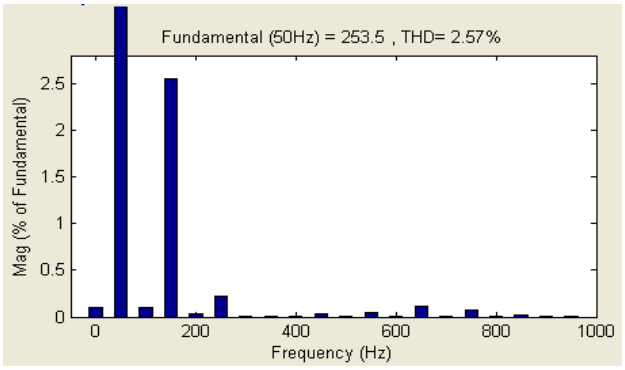


Fig 28: THD of Seven Level Output Voltage With Filter

Conclusion

Multilevel converters can achieve an effective increase in overall switch frequency through the cancellation of the lowest order of switching frequency terms and also reduce the harmonic components so that it can increase the power quality in power distribution system. The simulation results for five level inverter and seven level inverter has been implemented and its principle of operation has been confirmed by simulations results. MATLAB/SIMULINK model is developed and simulation results are presented. Whenever as our level increases we get pure sine waveform as per IEEE standards, the THD value is less than 5% and we get 2.45% , nothing but harmonic free response. Today, worldwide research and development of multilevel inverter-related technologies are going on. The focus of this paper is limited to fundamental principle of different multilevel inverters, modulation technique, and harmonic analysis to improve the power quality.

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