

Research Article

Performance Analysis of Router for Network on Chip

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Abstract

Major drawback of bus based communication system is that the loading effect becomes more if the complexity of the system is increased which drops the speed further. Ad-hoc routing of wires results in backend complications, lower performance and higher power consumptions. Network on Chip (NoC) has been adopted as a new promising solution for its extensibility and power efficiency. The fundamental unit of Network on Chip is the router. In this paper, we proposed a router module with wormhole switching concept. The router module is described at RTL level using VHDL and simulated in Xilinx ISE 13.1 simulator.

Keywords: System on Chip, Network on Chip, Routers, Switching Techniques, Arbitration.

1. Introduction

With the continuous advancement of the semiconductor technology will intimate us to integrate billions of transistors on a single chip resulting in many different processing elements on a single chip called System on Chip (SoC). In the past, mostly bus based communication architectures were used to connect the individual components of a system-on-chip (SoC) (M. Mitic et al 2006). A new interconnects architecture for future SoC designs is based on a number of small switching components inside the device (A. Brinkmann et al 2002). Packet switched network on chip implemented on FPGA is efficient solution for the SoC interconnect problem. Thus as mentioned in (S. Furber et al 2005), to overcome the problems of complex SoC interconnect design, packet switched Network on Chips (NoCs) are most approaching technique. In recent years, NoC architecture is adopted as a good alternative to ancient interconnection structure having flexibility, scalability; lower power consumption and better performance. A NoC can be described by its topology and by the method used for buffering, switching, routing, flow control and arbitration. The NoC architecture, as shown in figure 1, comprises of components such as routers, physical channels and network interface. A care must be taken while designing router because it is the core communication medium. Routers are connected with each other by a parallel channels to form a network topology like mesh or torus. Its role is to forward data packets from source to

destination port in the network. All routers are said to dissipate significant idle state power. The additional energy required to route a packet through the router is then shown to be dominated by the data path (A. Banerjee et al 2009). The major thrust behind the evolution to NoC based solutions is the inadequacy of current day VLSI inter-chip communication design methodology for the deep sub-micron chip manufacturing technology (K. Latif et al 2010).

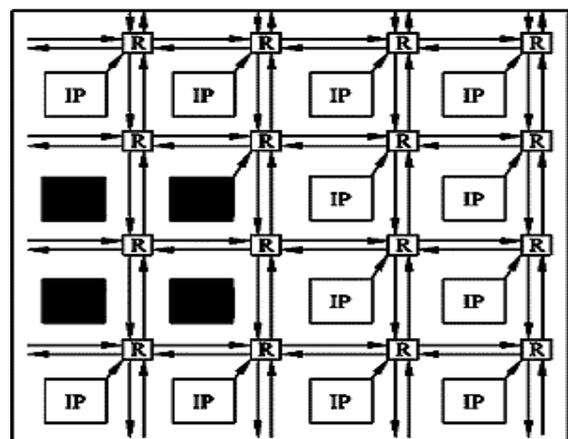


Fig. 1 Typical NoC Architecture

2. Related Work

Router design is not a recent issue but more attention should be paid while designing router as it can affect the overall performance of the NoC system. The flow control technique affects directly the buffer design. In flow control

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techniques such as Store and Forward, because the data unit is packet, a large buffer is needed and the buffer size depends on the packet size. The Wormhole flow control technique was proposed to improve the buffer utilization. In this, the smallest unit of flow control is flit (flow control digit) instead of packet as shown in Figure 2.

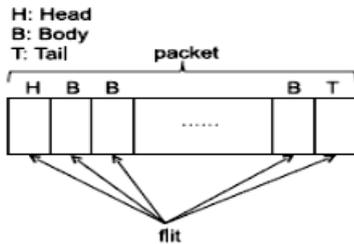


Fig. 2 Packet format

A packet consists of three types of flit: head flit, body flit and tail flit. The head flit contains control data such as routing information of the packet, the body flit contains transferring data and the tail flit indicates the end of the packet.

Arbab Banerjee compared different router architectures and it was concluded that wormhole routers dissipate significantly less power as compared to speculative virtual channel routers synthesized in a high performance TSMC 90nm technology.

Soteriou et al proposed distributed shared buffer (DSB) NoC router architecture, which shows a significant improvement in throughput at the expense of area and power due to extra crossbar and complex arbitration schemes.

The speculative virtual channel router was proved to have a very similar efficiency to the wormhole router with an increase in area by Khalid Latif.

The author proposed an area-efficient design for the router component of a NoC, i.e., the input block and the scheduler. It is proved that SRAM-based input blocks in place of synthesizable flip-flops have resulted in a saving of over 50% of the silicon area.

3. Router Module

The VHDL design of a router for a 2D mesh NoC is presented here. It works with XY routing algorithm. The router has five input and five output ports. The basic router has three main components: input port, arbiter, and crossbar, as shown in Figure 3.

The router has input buffers only because wormhole packet switching is selected. In addition to the wormhole switching technique, a router can be connected to its neighbors by bidirectional NEWS (North, East, West, South) links. Data packets between immediate neighbor routers are exchanged by the NEWS link.

The input port for each direction is responsible for handling, storing, and processing of each incoming data. It consists of a FIFO buffer to store the data and control logic to process it. The FIFO receives read and write requests from each direction. When the FIFO is full, write operations are disabled and when it is empty,

read operations are disabled. The FIFO empty flag is set to high when the FIFO is empty and the full flag is set to high when the FIFO is full.

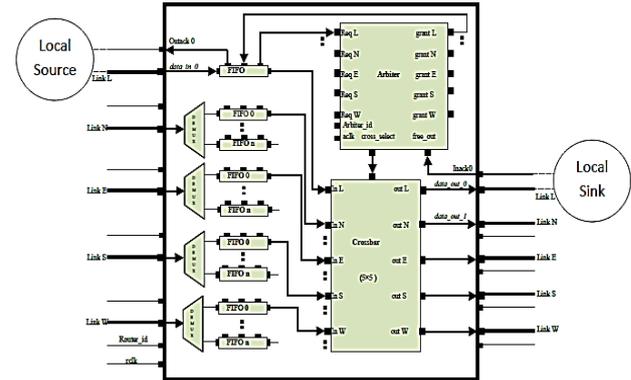


Fig. 3: 5 x 5 Wormhole Basic Router

The arbiter allows the output ports to request input ports in a router. The global switch arbiter, which contains five arbiters, receives requests from the routing function of each input port and assigns available output ports to the requestors, resolving contention. Arbiters used in this work employ the round-robin algorithm. Each arbiter has as input 4 concurrent requests sent by the routing module of other input ports. Only one request is granted by the arbiter, and the output port is allowed to the input port winner.

The arriving packets that have been granted passage on the crossbar are passed to the appropriate output channel. The connection between an input port and its associated output port is accomplished by the crossbar switch, which is also arbitrated by the arbiter. Figure 4 shows the flow chart to transmit a flit. The router model receives an incoming flit from the source and forwards it in the desired direction of travel. As the machine is initialized, it waits for a flit to be ready to send and then waits for the destination to become available and transmits the flit onwards. After transmitting the flit, it acknowledges the sender node about the transmission end.

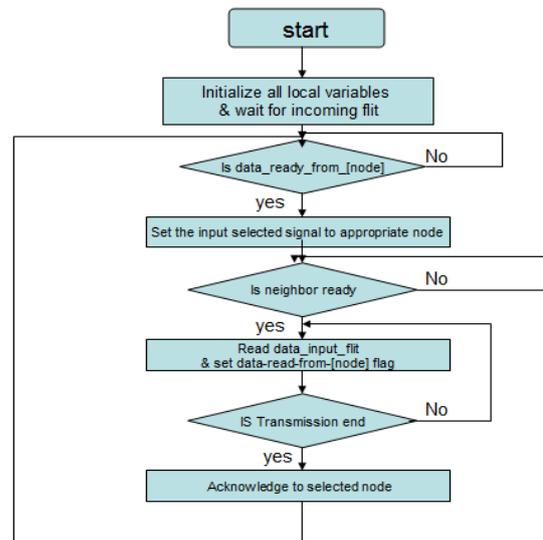


Fig. 4 Flow chart to transmit data

4. Simulation

A. Simulation Environment

We have simulated the base router and wormhole concept router in VHDL. The target FPGA device is the Xilinx Spartan3 xc3s200-5ft256 with 19220 slices. The Xilinx ISE 13.1 is used to synthesize the router code.

B. Simulation Result

Each node has an input port consists of FIFO buffers, one for each input link, and a mechanism to connect inputs to outputs. Each of these buffers can store four flits belonging to the same message. The minimum input arrival time before clock is 12.385 ns and maximum output time required time after clock is anticipated as 6.306 ns. The maximum frequency of this router is estimated as 100.944 MHz. Table I show the resource utilization of the NoC router module in FPGA.

Table I Resource Utilization of Router module in FPGA-Xilinx (DEVICE- xc3s200-5ft256)

Resource	Available	Used	% Utilization
Slices	19220	688	35
Slice Flip Flops	3840	415	10
4 Input LUTs	3840	1279	33
Bonded IOB	173	126	72
GCLK	8	1	12

Conclusions

A router using wormhole concept is proposed in this paper. The synthesis and simulation of the proposed router is demonstrated through VHDL codes using XILINX ISE

13.1 software. The simulation makes possible understanding of routing pattern and the concept of wormhole switching technique of the router for a network on chip. In future, we have it in mind to work on improving the scheduling algorithm used in the router for better performance.

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