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Research Article

A Comparative Delay Analysis of Copper Interconnect with Future Candidate CNT

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Abstract

Development in VLSI technology leads to various futuristic possibilities as well as various design challenges for ICs. With a pace of time technology of copper interconnect suffers from various problems such as power dissipation, delay, cross talk etc. In order to meet the demand of futuristic technology of interconnects a promising alternative solution comes out to be carbon nanotube (CNT). In this paper a comparative analysis is made to investigate the problems of interconnect that are facing by current technology i.e. copper interconnect and to identify its alternative solution scope for the interconnect problem by comparative analysis. In this paper traditional copper interconnects are compared to new innovative interconnect that is made by bundles of single wall carbon nanotubes. The delay the performance of the CNT –bundle and copper interconnects was compared respectively at local, intermediate and global lengths.

Keywords: *Interconnect, Copper (Cu), Carbon Nanotube (CNT), Single wall Carbon Nanotube (SWCNT),Multi wall Carbon nanotube(MWCNT),Resistance Capacitance(RC)*

1. Introduction

The performance improvements and advancement in VLSI technology leads to shrink of chip size from µm to nm. But with this advancement it also leads to several other problems too, out of which interconnect problem is one of the dominating factor that affect the performance of Chip. Not only do interconnects become more important, but they also become much more difficult to model and optimize in the deep submicron VLSI technology.

With shrink in technology the copper interconnect facing problem to cope up with current interconnect requirement as with decrease in size it suffers from various problems. The resistance of copper interconnects, with cross-sectional dimensions close to the order of the mean free path of electrons in current and imminent technologies, is increasing rapidly under the combined effects of enhanced grain boundary scattering, surface scattering and the presence of the highly resistive diffusion barrier layer. The steep rise in parasitic resistance of copper interconnects cause serious challenges for interconnect delay (especially at the global level where wires have long distances) and for interconnect reliability hence it has a significant impact on the performance and reliability of VLSI circuits. As the transition from aluminum to copper some years back takes place similarly to eliminate current problems change in the material of interconnect have to be soughed. Thus to fulfill the demand of future interconnects carbon nanotube comes out to be most promising alternative solution. Carbon nanotubes have been recently proposed as a possible future replacement for metal interconnects in future technologies. Carbon nanotubes are made from graphene sheets by rolling up them in cylindrical form. The diameters of these cylinders are of the order of a nanometer. Depending on the fact that on which direction CNTs are rolled up (chirality), they demonstrate either metallic or semi-conducting properties. For interconnect application metallic carbon tubes fulfill the desire requirements. There are two types of CNTs, Single walled CNT (SWCNT) and Multiwall CNT (MWCNT). CNTs that contain only one thin wall of graphene sheet are SWCNTs. There are some CNTs which consist of a multiple of concentric SWCNT like graphene tubes. These are termed MWCNT. Because CNT exhibits desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity (DavoodFathi*et al*, 2007), CNTs have aroused a lot of research interest in their applicability as VLSI interconnects for future. However, the high resistance associated with an isolated CNT (greater than 6.45 KΩ) necessitates the use of a bundle (rope) of CNTs conducting current in parallel to form an interconnection.

In this paper we compare copper interconnect with carbon nanotube which offer important guidance regarding

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the carbon nanotube technology development which is required for improving interconnect performance. Our work is aimed to provide appropriate information regarding existing literature and its future scope.

2.Background of Copper Interconnect

With rapid growth of VLSI technology, the number of on-chip interconnects is on the rise. To accommodate more interconnects, the cross-sectional dimensions are reduced rapidly resulting in dimensions of the order of mean free path of electrons in copper which leads to increase the resistivity of interconnect. As the interconnect size is scaled down, the resistivity of the copper increases mainly due to grain and surface scattering effects. This effect along with the higher current densities requirement that must be carried by the future interconnects makes the copper interconnects more and more vulnerable to electro migration failure in the near future. As a result of these effects together with increase in interconnect resistance with length enhances delay. To understand the trend of increasing resistivity, we look at the ITRS roadmap. From ITRS reports, (ITRS *et al*, 2007) we find that the copper resistivity for future technologies is increasing at a very fast rate as shown in Fig.1

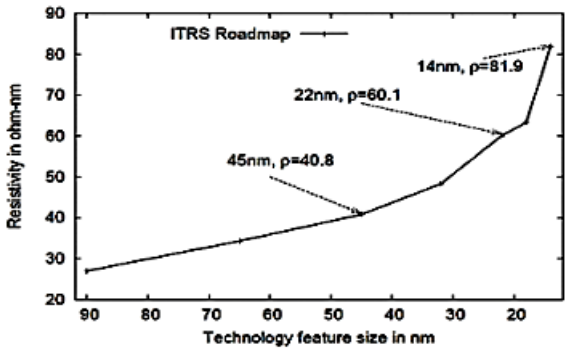

Fig.1 Resistivity increase from ITRS roadmap. There is a steep increase in resistivity as we move into 22nm and lower technology node.(ITRS *et al*, 2007)

Besides the increase in delay, interconnect power dissipation also increases because of increased current density and frequency of operation. The increased heating due to the rise in power dissipation lead to assists electro migration. Such scaling dependent limitations of copper interconnect is going to be more and more severe for the future generation of VLSI chips.

The parametric analysis of copper and SWCNT bundle as interconnects for VLSI circuit is done in this section. Using these parameters, the performance of CNT bundle interconnects is compared to copper wires.

3. Interconnect Modeling Parameters

To study and understanding the behavior of CNT and copper interconnect it is required to study their parameters. Using these parameters, parasitic effect on the performance of CNT bundle interconnects is compared with copper interconnect at local, intermediate and global level.

3.1 Modeling Parameters of Copper Interconnect(BPTM et al, 2010)

3.1.1 Resistance

$$r = \frac{\rho l}{wt} = \frac{(\rho_s + \rho_g)}{wt} l \quad (1)$$

where the resistivity ρ takes into account the effects due to surface scattering and grain boundary scattering. Expression for the resistivity is given by

$$\frac{\rho_s}{\rho_0} = 1 + \frac{3}{4}(1-p)\frac{l}{w} \quad (2)$$

$$\frac{\rho_g}{\rho_o} = 3\left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 ln\left(1 + \frac{1}{\alpha}\right)\right] \quad (3)$$

where

$$\alpha = \frac{l}{d} \times \frac{R}{1} - R$$

3.1.2 Capacitance

$$C_g = \varepsilon\left[\frac{w}{h} + \left\{2.22\left(\frac{s}{s+0.7h}\right)^{3.19}\right\} + \left\{1.17\left(\frac{s}{s+1.51h}\right)^{0.76}\left(\frac{t}{t+0.7h}\right)^{0.12}\right\}\right] \quad (4)$$

Where ε_o is the dielectric permittivity; and ε_r is the relative dielectric permittivity of copper

$$\varepsilon = \varepsilon_r \times 8.86 \times 10^{-12} \quad (5)$$

Thickness t is determined by t = 3 × W (width of interconnect),s is the space between wires (assumed s=w), h is the height of the wire (h=w × aspect ratio).

3.2 Modeling Parameters for SWCNT Interconnect

3.2.1 Resistance

An isolated CNT resistance comprises of mainly three components: (1) Fundamental resistance of 6:45k-Ω (2) Scattering resistance (3) Imperfect metal nanotube contact resistance. If the wire have mean free path less than 1μm then its resistance is independent of wire length but if it have mean free path greater than 1μm then it resistance increase with length due to scattering phenomena(A. G. Chiariello *et al*,2009). Thus overall resistance of an isolated CNT wire (length > 1μm) can be written as

$$R_{CNT} = \left(\frac{h}{4e^2}\right)\frac{L}{\lambda} \quad (6)$$

Were λ is the mean free path, L is length of nanotube and $(h/(4e\text{^}2) = R_F$which is quantum resistance of bundle. If length < 1μm, then resistance is given by quantum

resistance (h/(4e^2). In actual practice, the observed resistance of a CNT is much higher than the resistance derived above. This is due to the fact that presence of imperfect metal-nanotube contacts which give rise to an additional contact resistance.

3.2.2 Capacitance

CNT interconnect have three types of capacitance, first is quantum capacitance (C_Q), second is electrostatic capacitance above ground plane (C_E) and last one is *electrostatic* capacitance with any adjacent SWCNT (C_{EC}). The quantum capacitance (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Considering this energy an effective quantum capacitance (per unit length) may be obtained which is expressed by

$$C_Q = \frac{2e^2}{hv_f} \approx 100 \frac{aF}{\mu m} \quad (7)$$

wherev_f is the Fermi velocity in graphite and is approximately 8×10^5 m/s(Barry J. Cox*et al*,2007).Because of four conducting channels in CNTs, the total effective quantum capacitance that results from four parallel channel is 4CQ.The electrostatic capacitance (C_E) is due to charge stored by the CNT above ground plane system and is given by

$$C_E = \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)} \quad (8)$$

where 'd' is the diameter of CNT, over a ground plane at a distance 'y' below it. Similarly, we can get the electrostatic capacitance per unit length between two parallel SWCNTs as:

$$C_{EC} = \frac{\pi\varepsilon}{\cos^{-1}\left(\frac{s}{d}\right)} \quad (9)$$

where s is the inter-SWCNT spacing and d_t is the SWCNT diameter.

3.3 Modeling Parameters for SWCNT Bundle Interconnect

The number of SWCNTs in a bundle is given by (C. Thiruvenkatesan*et al*, 2009)

$$n_{CNT} = n_w n_H - \frac{n_H}{2} \quad \text{if } n_H \text{ even} \quad (10)$$

$$= n_w n_H - \frac{n_H - 1}{2} \text{ if nH odd} \quad (11)$$

were

$$n_w = \left[\frac{w-d}{x}\right] \quad (12)$$

$$n_H = \left[\frac{h-d}{\left(\frac{\sqrt{3}}{2}\right)x}\right] + 1 \quad (13)$$

where, $n_w$is the number of columns in a bundle, $n_h$is the number of rows in a bundle, and $n_{CNT}$is the number of SWCNTs in a bundle.

3.3.1 Resistance

The resistance of a CNT bundle is simply the quantum resistance divided by n_{CNT}.

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} \quad (14)$$

were $R_{isolated}$ = resistance of single SWCNT

3.3.2 Capacitance

SWCNT has two capacitance components: electrostatic (C_E), and the additional quantum capacitance (C_Q) (C. Thiruvenkatesan*et al*, 2009) due to a reduced 2-D density of states for electrons. To add an electron in a SWCNT, one must add it at an available quantum state above the Fermi energy (EF) due to the Pauli's exclusion principle. C_E and C_Q can be described as eq (6) and (7) respectively

$$C_E^{bundle} = 2C_{En} + \frac{n_W - 2}{2} C_{Ef} + \frac{3(n_H - 2)}{5} C_{En} \quad (15)$$

$$C_Q^{bundle} = C_Q^{CNT} n_{CNT} \quad (16)$$

C_E^{bundle}= total electrostatic capacitance

C_Q^{bundle} = quantum capacitance of bundle

n_{CNT}= total no. of CNT forming bundle

Total Effective capacitance of series combination is

$$\frac{1}{C_{bundle}} = \frac{1}{4C_Q^{bundle}} + \frac{1}{C_E^{bundle}} \quad (17)$$

And capacitance per unit length is given by (H.Aghababa*et al*, 2008)

$$C = C_{bundle} l \quad (18)$$

4. Delay analysis of CNT bundle with Copper

Delay in VLSI circuit is defined as the difference in the time when the output waveform crosses 50% of its final value and its corresponding time for the input waveform. The delay in VLSI circuit can be calculated in different ways. Here the popular Elmore delay expression is used to obtain the delay of CNT bundle and Cu interconnects.

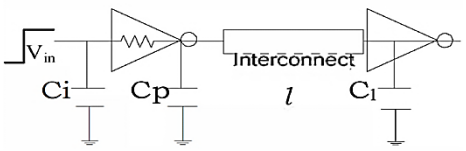

Fig.2 Schematic of CNT or Cu interconnect circuit used for performance evaluation of delay (H. Li*et al*, 2006)

The delay expressions for the equivalent circuit shown in Fig.2 for CNT bundle are

$$\tau_{CNT} = 0.69\left\{\frac{r_s}{n_{CNT}} + \frac{R_c+R_Q}{n_{CNT}}\right\}C_l + 0.69r_s(C_l + C_P) + 0.69\left\{r_s + \frac{R_c+R_Q}{2n_{CNT}}\right\}C^{bundle} \times l + 0.38\left(\frac{R_S}{n_{CNT}}\right)C^{bundle} \times l^2 \quad (19)$$

and for copper delay expression is

$$\tau_{Cu} = 0.69r_s(C_l + C_P) + 0.69r_sC_{Cu}l + 0.38R_{Cu}C_{Cu}l^2 + 0.69R_{Cu}C_l l \quad (20)$$

r_s = driver resistance

C_l= load capacitance

C_p = parasitic capacitance

C^{bundle} = bundle capacitance

C_{cu} = Capacitance of Cu

R_{cu} = Resistance of Cu

5. Comparative Delay Analysis Of SWCNT bundle Interconnect with Copper interconnect based On Parameters Described Previously

On the basis of parameters discussed in previously section of CNT bundle and Copper interconnect, delay is determined by using equations (18) and (19). Parasitic values of equivalent resistance, capacitance and inductance of Bundled CNT and copper interconnect are put in their respective delay expression to determine the delay that are obtained byconsidering the geometries suggested in (SudeepPasricha*et al*, 2009) (N. Srivastava*et al*, 2005) for 22nm. and then compare for analysis for local, intermediate and global level.

Delay analysis for local Interconnect

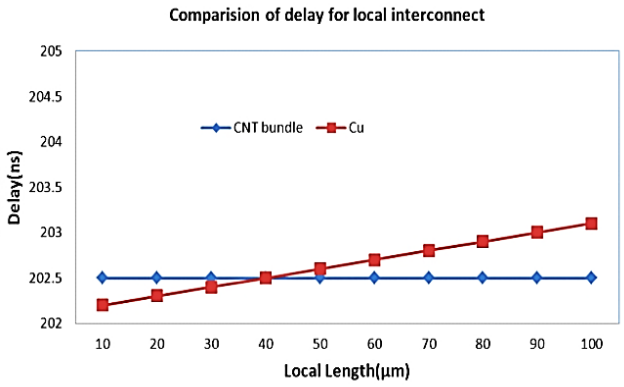

Fig.3 Comparison of delay among the SWCNT bundle and Cu interconnects for local length.

Delay analysis for semiglobal Interconnect

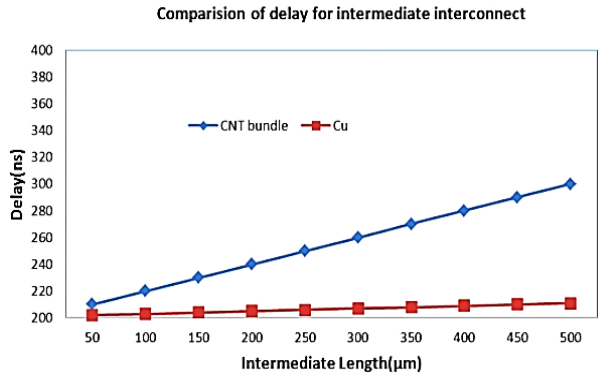

Fig.4 Comparison of delay among the SWCNT bundle and Cu interconnects for intermediate length.

Delay analysis for global Interconnect

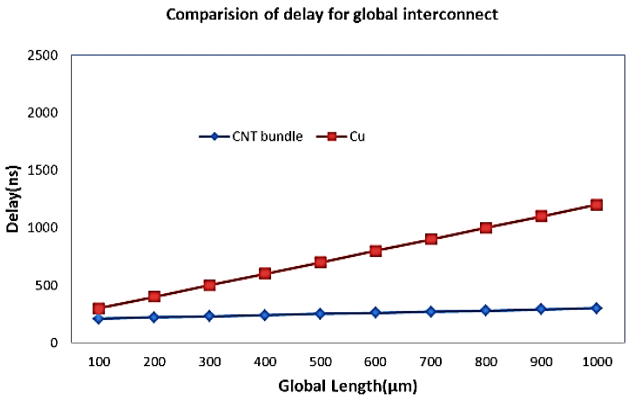

Fig.5 Comparison of delay among the SWCNT bundle and Cu interconnects for global length.

Thus from figures 3, 4 and 5 we observe that in the case of local length the delay of bundle of SWCNT tends to decrease after a certain length than Cu interconnects but in the case of intermediate and global length it gives tremendous result than Cu interconnects. The main reason for such phenomena is the fact that it mainly arises due to the fact that the effective resistance capacitance (RC) product of SWCNT bundle at hexagonal shape is lower than single copper and gold interconnects. Beside this circuit based fact the physical one dimensional structure with a little electron surfacescattering and grain boundary scattering is also underlying fact of this result.

5. Conclusion

In this paper we have compared delay performance metrics of a CNT bundle with Copper interconnect for local, semi-global and global interconnects at 22nm technology node. To analysis delay we use Elmore delay expression to obtain the delay of CNT bundle and Cu interconnects. For local, semiglobal and global

interconnects, we have compared the performance of existing Cu wire with a CNT bundle based novel wire For local interconnects, CNT yield comparable latency to copper, but in the case of intermediate and global length it gives tremendous result than Cu interconnects. In general, the CNT bundle shows lower latency than Cu.

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