International Journal of Current Engineering and Technology
ISSN 2277 - 4106
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Research Article

Two Neuron Model for Voltage Flicker Mitigation Using Generalized Unified Power Flow Controller

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Accepted 8 April 2012, Available online 1June 2012

Abstract

Electric power quality broadly refers to maintaining a near sinusoidal bus voltage at rated magnitude and frequency. Due to the advancement and proliferation of information technology and the widespread use of power electronic devices in recent years, utilities' customers in various industrial fields are suffering economic losses from short interruptions and voltage flickers. The FACTS devices like SVC's, STATCOM, UPFC and DVR have been able to solve the voltage flicker problems by rapidly controlling the reactive power. In the case of two different sensitive loads in an industrial park fed from two different feeders with different voltage levels, protection from voltage flicker can be done by two DVRs having common dc link called IDVR. But in case when the lines are connected with same grid substation and feeding two different sensitive loads in an industrial park, voltage flicker in one line affects the voltage profile of other lines. Under the above circumstances, voltage flicker cannot be mitigated by IDVR due to insufficient energy storage in dc-link. This paper proposes a voltage flicker compensator based on generalized unified power flow controller (GUPFC), which comprises of three voltage-sourced converter modules sharing a common dc link. Two voltage-sourced converter modules connected in series with the lines, compensate voltage flicker and a third shunt converter module maintains bus voltage and replenishes the common dc-link energy storage. The control strategy for power flow control of shunt converter and flicker compensation control of series converters are derived. This work evaluates the performance of the above compensating device with the proposed algorithm called two neuron control algorithm for simultaneous flicker compensation and replenishing dc bus energy. This algorithm uses the simplest pre-sag supply voltage boosting technique. Besides, a self-charging technique is used which maintains the dc capacitor voltage at the desired level. Since the controls do not include any parameter which is dependent on network condition, the performance of such controller is robust with respect to network structure, flicker location and system loading. The control structure is decentralized and does not need any coordination with other compensating devices. The structure of proposed algorithm is easy to understand, easy to implement and attractive from a view-point of engineering. The model is simulated in MATLAB/SIMULINK platform and GUPFC controller's performance is evaluated. Numerical simulation proved the effectiveness of the GUPFC with two neuron model in compensating voltage flicker.

Keywords: *Voltage flicker, power quality, Two neuron control algorithm, generalized unified power flow controller (GUPFC), self-charging technique.*

1. Introduction

A modern consumer requires high quality power supply for their sensitive loads. Voltage flicker has become an important power quality issue. It is reported that a small voltage fluctuations of less than 0.5% in the frequency range of 5-10 Hz can cause visible lamp voltage flicker (M. Bollen et al., 2006). The main sources of voltage fluctuations can be divided into two main categories which are step voltages changes in regular time interval and cyclic voltage changes. Loads that lead to voltage fluctuations are arcing furnaces, welding machines, rolling mills, mine winders, large capacitor bank used for power factor improvements and electric boilers. An example of a low voltage load that leads to voltage fluctuations are copying machine, X-ray equipments, drives for lifts, pumps, fans, refrigerators and electric cookers (R. C. Dugan, et al., 2006). In certain circumstances, superimposed inter harmonics in the supply voltage can lead to oscillating luminous flux. Sources of inter harmonics which are responsible for flickers, include static frequency converters, sub-synchronous converter, induction machines and arc furnaces (Angelo Baggini.P, 2008). Voltage flicker affect motor starting results in temperature rise and motor overloading. It affects control systems; reduce the lifetime as well as degradation of performance of the electronic, incandescent, fluorescent

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and CRT devices. It has been also observed that the voltage fluctuations led to small speed variations of electrical motor results in variations in final quality of products (J. A. Arrillaga et al., 2008). The voltage variations and mitigation studies for equipments like arc furnaces, electric welders, motors, generators and wind turbines, can be found in (M.M. Morcos, et al., 2005). In (J.Jatskevich, et al., 2008), the UIE/IEC flicker meter for flicker measurements and adaptive VAR compensator (AVC) model has developed. Using line current measurements, instantaneous voltages were estimated and a state estimation method for monitoring the voltage flicker have been proposed in (Mahmoud Mazadi at al., 2009). In (Weihao Hu et al., 2009), the authors have proposed a new method of voltage flicker mitigation by controlling active power for variable speed wind turbine. The flicker measurements and effective mitigation methodologies can be studied in (Garcia-Cerrada A et al., 2000; Z. Zhang et al., 2001). The limits of flicker emission for an individual fluctuating load must be determined in order to assure that the total flicker injection from all types of loads does not exceeding the planning levels. Procedure for determining the requirements for connecting large fluctuating loads to MV and HV levels are explained in IEC 61000-3-7. Flicker emission planning levels provided by IEC must be always less than or equal to the compatibility levels for LV and MV systems. The IEC 61000-3-3 provides and explains voltage flicker emission limits for the equipments connected to LV systems. The standard IEC 61000-4-15 gives the functional and design specifications for flicker measurement apparatus to indicate the correct flicker perception level for all practical voltage fluctuation waveforms. In this, the overall response from the instrument input to output is given for a sinusoidal and rectangular voltage change at frequencies between 0.5 and 25 Hz. It also includes a performance test to define a set of rectangular voltage changes of different frequencies and depths for which the short time flicker severity, P must be 1.00 ± 5 %.It includes standard models for 230 V, 60 W and 120 V, 60 W lamps. The flicker meter can be used to for the loads that are already in operation. However, direct measurement using flicker meter cannot be applied in the design or planning stage of an installation. In these cases, some analytical methods are required so that flicker severity level should not exceed than the planned level. Such analytical method also helps in determining and finalizing mitigation methodology (Walid G et al., 2009). The IDVR (D. Mahinda Vilathgamuwa et al., 2008) scheme provides a way to transfer real power between sensitive loads in individual line through the common dc link of the DVRs, as it does in the Interline Power flow Controller (IPFC). However, the lines in the IPFC originate from a single grid substation while the lines in the IDVR voltage sag by importing real power from the dc link, the other DVRs replenish the dc-link energy to maintain the dc-link voltage at a specific level using Current source Inverter (Dong Shen et al., 2002). An example of a potential location for such a scheme is an industrial park where power is fed from different feeders connected to different grid substations, those that are electrically far apart. The sensitive loads in this park may be protected by DVR connected to respective loads. The dc links of these DVRs can be connected to a common terminal, there by forming an IDVR system. This would cut down the cost of the custom-power device, as sharing common dc link reduces the size of the dc-link storage capacity substantially, compared to that of a system in which loads are protected by clusters of DVRs with separate energy storage systems. This IDVR works efficiently when the lines under consideration are connected with two different grid substations, as it is reasonable to assume that voltage flicker in one line would have lesser impact on the other line. But in case when the lines are connected with same grid substation and feeding two different sensitive loads in an industrial park, voltage disturbance in one line affects the voltage profile of other lines. Under the above circumstances, voltage flicker cannot be mitigated by IDVR due to insufficient energy storage in dc-link. This paper proposes a voltage flicker compensator based on generalized unified power flow controller (GUPFC), which comprises of three voltage-sourced converter modules sharing a common dc link. Two voltage-sourced converter modules connected in series with the lines, compensate voltage flicker and a third shunt converter module maintains bus voltage and replenishes the common dc-link energy storage. The control strategy for power flow control of shunt converter and flicker compensation control of series converters are discussed in detail. Adjustable carrier PWM is used for generating switching pulses. The simulation model of GUPFC is developed in this work. The salient advantages of the proposed method are compensating long duration deeper voltage sags, reduction in size of dc-link capacitor and simultaneous voltage sag compensation in all lines.

2. Pre-sag voltage boosting technique

The basic principle of pre-sag voltage boasting technique can be used for flicker mitigation. In this compensation mode the load voltage is compensated to the nominal supply voltage as shown in figure 1. The real power delivered by DVR1 to load can be written as in equation (1).

$$P_{DVR1}=V_1 I_1 (3pf_1 M\cos(\varphi+\vartheta)) \quad (1)$$

Where, $S_1=3V_1I_1$; $\mathrm{a}_j = \dfrac{V_{s1j}}{V_1}$

$$X = \sum_{j=1}^{3} \mathrm{a}_j \cos(\delta_j)$$

$$Y = \sum_{j=1}^{3} \mathrm{a}_j \sin(\delta_j)$$

$$M = \sqrt{X^2 + Y^2}$$

$$\theta = \tan^{-1}\left[\frac{Y}{X}\right]$$

P_{DVR1} is the real power supplied by DVR1, a_j is the flicker factor, δ_j is the phase angle jump, ϕ_1 is line-1 PF angle, I_1 is line-1 load current, V_1 is load voltage of line-1 and V_{s1} is the supply voltage of line-1

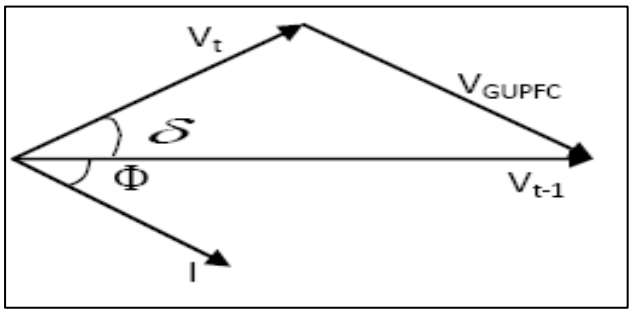

Figure 1 Pre-sag supply voltage boosting technique

Assuming a balanced voltage sag with sag factor a and phase angle jump δ, the phase advance angle β is given as,

$$\beta = \phi_2 - \cos^{-1}\left[\frac{S_1(pf_1 - a * \cos(\phi_1 + \delta) + P_{loss})}{S_2} + pf_2\right] \quad (2)$$

As flicker factor depends on phase angle jump δ and δ is not controllable, DVR1 operating in pre-sag supply voltage boosting technique generally requires significant number of lines to be connected to the common dc link in order to mitigate flickers.

3. GUPFC in voltage flicker compensation

The generalized unified power flow controller consists of three voltage sourced converters. Two converters are connected in series with the transmission lines called series converter and the third converter is connected in shunt with the sending end bus called shunt converter. In other words, the GUPFC comprises of two static synchronous series compensators (SSSC) and a static compensator (STATCOM). However, the compensating converters are linked together at their dc terminals, as illustrated in figure 3. With this scheme, in addition to providing series reactive compensation, series converters can be controlled to supply real power to the common dc link from its own transmission line. The shunt converter can be used for controlling the bus voltage as well as to maintain constant dc-link voltage. The series converters can be operated to inject the desired voltage into the lines. There are four variables associated with the series converters viz. voltage magnitudes and phase angle of injected voltage in both lines. Both the voltage magnitude and phase angle of injected voltage on both the lines can be controlled independently such a way to maintain flicker free load voltage. The amount of real power transferred by the series converters to the lines should be equal to the amount of real power transferred by the shunt converter from bus to dc-link energy storage. The power balance equation can be written as in equation (3).

$$P_{ex} = C_o V_{DC} \frac{dV_{DC}}{dt} - P_{Series1} - P_{Series2} + P_{loss} \quad (3)$$

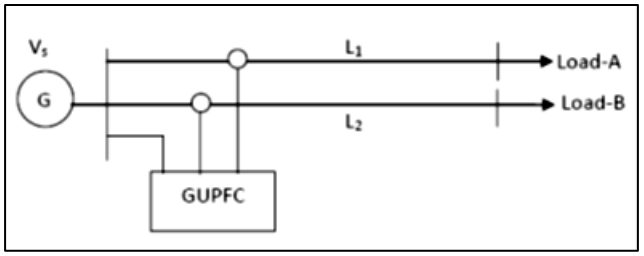

Fig. 2 Basic connection of GUPFC

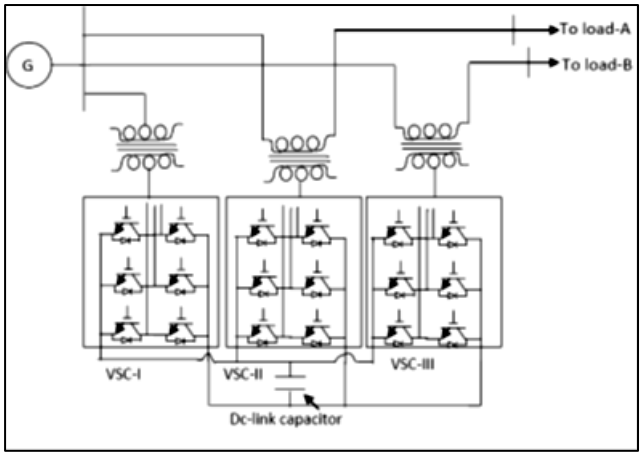

Fig. 3 Basic structure of GUPFC

It is clear from equation (2) that the real power exchanges between lines through the common dc link takes place in a nonlinear fashion. Thus, by sensing the voltage on the dc link and comparing it with a reference dc-link voltage, a controller can regulate the real power flow and maintain the required voltage level in the dc link. In the transient condition such as the beginning of operation of series converters, the initial transient energy is supplied by the dc-link capacitor until the voltage controller of shunt converter regulates it. Therefore, the size of dc link has to be determined so that the dc-link voltage drop is limited to an allowable minimum value.

The basic connection of generalized unified power flow controller is shown in figure 2, which shows the single line diagram of a system which has two transmission lines L_1 and L_2 which feeds load A and B respectively. The GUPFC is installed near the sending-end bus in the system. The circuit model is shown in figure 4. The series converter modules of GUPFC connected to the transmission line are modeled as variable voltage sources V_{11} and V_{12}. The shunt converter module is modeled as current source I_{sh}. The series impedance of the lines is represented as Z_{sc1} and Z_{sc2}. The impedance of the loads is denoted as Z_{L1} and Z_{L2}. The source voltage is V_s and its impedance is Z_s. The shunt converter module is controlled such a way to maintain dc link voltage and bus voltage at the desired level. In this work, the bus voltage control is not incorporated. This control is referred as power flow control mode. The series converter modules are controlled such a way to mitigate voltage flicker. The control strategies are explained in the following section.

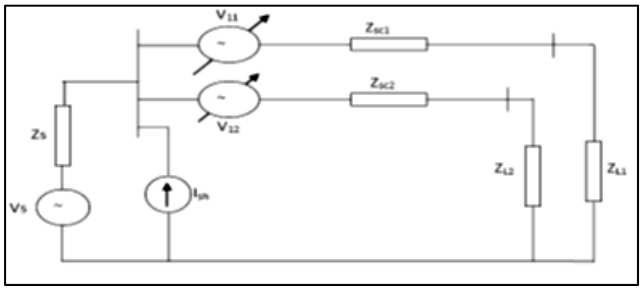

Fig. 4 System model

4. Control strategy of GUPFC

The control strategy derived for maintaining dc-link voltage of shunt active filter is applied here, for maintaining the dc-link energy storage of GUPFC. A simple control algorithm is developed which does not use PI controller. To regulate the dc link capacitor voltage at the desired level, an additional real power has to be drawn by the GUPFC from the supply side to charge the two capacitors. The configuration of three-phase self-charging current is shown in figure 5. The PLL synchronizes itself with the supply voltage of phase 'a' and outputs three sine waves which are 120° out of phase from each other. Three phase i_{dc} is obtained by multiplying these sine waves with the current I_{dc} which is calculated by the control algorithm. Thus, the three phase injection currents can be calculated as

$$i_{inj,a} = -I_{dc}\sin\omega t$$
$$i_{inj,b} = -I_{dc}\sin(\omega t - 120)$$
$$i_{inj,c} = -I_{dc}\sin(\omega t + 120) \quad (4)$$

Where I_{dc} is given as

$$I_{dc} = 2C\frac{\left\{[V_{dc}(ref)]^2 - [V_{dc}]^2\right\}}{3VT} \quad (5)$$

The minus sign indicates that the charging current idc flows into the GUPFC. An adjustable carrier PWM controller is used to control the switching of the GUPFC.

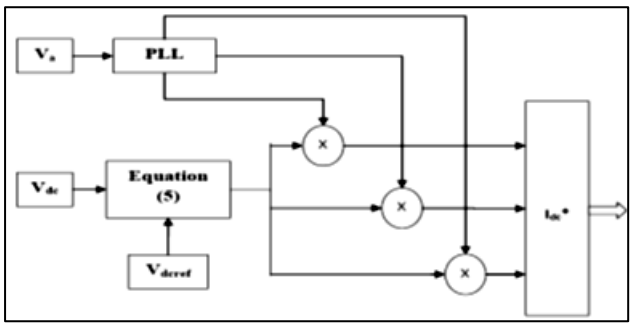

Fig. 5 Three-phase self-charging circuit

The simplest pre-sag supply voltage boosting technique is considered for developing a new two neuron control algorithm. The pre-sag voltage boosting technique can be explained by vector diagram shown in figure 1. This algorithm can also be applied for flicker mitigation. Current is taken as reference vector throughout this section. Under pre-flicker condition, the system voltage is V_{t-1} which leads current by an angle ϕ. At time't', flicker occurs in supply voltage and is shifted in phase by an angle δ called phase angle jump. The ratio of voltage during flicker to voltage before flicker is referred as flicker factor 'a'. That is, $a = V_t / V_{t-1}$. The series converter of GUPFC has to inject a voltage 'V_{GUPFC}' such a way to bring voltage during flicker V_t to its pre-flicker value V_{t-1}. The control algorithm developed for generating the reference signal to compensate voltage sag is named as two-neuron control technology. The control law is given as $V_{\alpha ref} = \gamma_1 V_\alpha$ and $V_{\beta ref} = \gamma_2 V_\beta$, where γ_1 and γ_2 are constants which are interpreted weights in the two-neuron model. $V_{\alpha ref}$ and $V_{\beta ref}$ denote the components of reference voltage in-phase and in phase-quadrature with line current respectively. The magnitude and angle of reference voltage can be calculated as,

$$|V|_{ref} = \sqrt{V_{\alpha ref}^2 + V_{\beta ref}^2} \quad (6)$$

$$\theta_{ref} = \tan^{-1}\left(\frac{V_{\beta ref}}{V_{\alpha ref}}\right) \quad (7)$$

The basic block diagram of the control algorithm is shown in figure 6. The input processing block and pre-flicker voltage generation block performs the same function of calculating the in-phase and phase-quadrature components of voltage, but for different input quantities. Figure 7 shows the input processing / pre-flicker voltage generation block. In case of input processing function, the inputs and outputs are $A=P_t$; $B=Q_t$; $C=V_t$; $D = V_\alpha$ and $E = V_\beta$. On the other hand, for pre-flicker voltage generation the inputs and outputs are $A=P_{t-1}$; $B=Q_{t-1}$; $C=V_{t-1}$;$D= V_{\alpha preflicker}$ and $E= V_{\beta flicker}$. The time lag block in figure 6 is used for obtaining inputs P_{t-1}, Q_{t-1} and V_{t-1} from P_t, Q_t and V_t respectively. The inputs are denoted in figure as shown in equation 8. Both input processing block and pre-sag voltage generation block responds to input only when activating signal is generated by the differentiator (figure 6). Under normal condition without voltage flicker, the differentiator output is zero and the blocks are not activated.

$$I_t = [P_t, Q_t, |V_t|] \quad and \quad I_{t-1} = [P_{t-1}, Q_{t-1}, |V_{t-1}|] \quad (8)$$

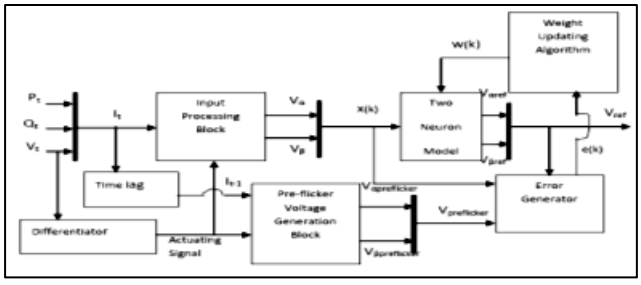

Fig. 6 Basic block diagram of proposed controller

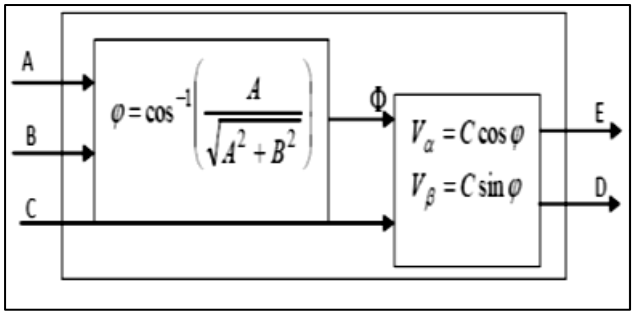

Fig.7 Input processing / Pre-flicker voltage generation

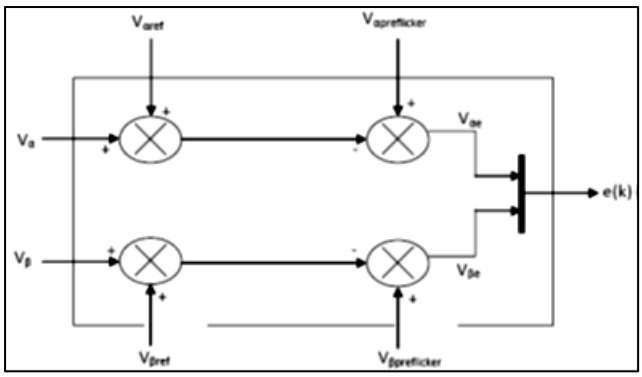

Fig. 8 Error generator

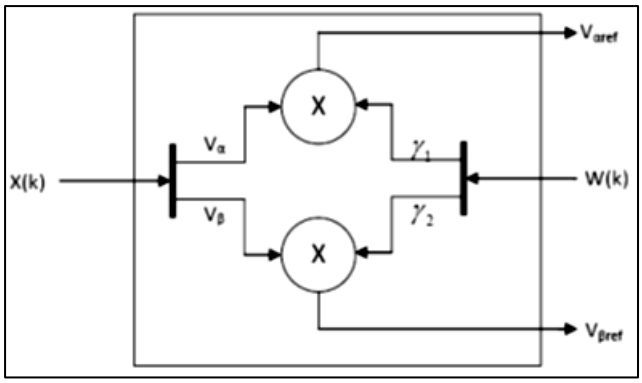

Fig. 9 Two-Neuron model

The error generator block is shown in figure 8. The line voltage is added with reference voltage generated by the control algorithm and compared with the pre-flicker voltage generated by pre-flicker voltage generation block. The error signal is given as input to weight updating algorithm. The error is given by

$$e(k) = \begin{bmatrix} V_{\alpha e} \\ V_{\beta e} \end{bmatrix} \quad (9)$$

The weight updating algorithm uses delta rule to update the weights of the two-neuron model. The weight vector is

$$W(k) = \begin{bmatrix} \gamma_1 \\ \gamma_2 \end{bmatrix} \quad (10)$$

The delta rule used for updating weights is

$$W(k+1) = W(k) + \frac{\alpha e(k) X(k)}{\lambda + X(k) X(k)^T} \quad (11)$$

where α is the reduction factor, γ is a constant chosen to be close to zero and is included only to avoid division by zero and X(k) is the input vector of the two-neuron model given as,

$$X(k) = \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (12)$$

The two-neuron model is shown in figure 9, which has two neurons and the activity of neuron is finding the product of input ($V_\alpha$and V_β) and weight (γ_1 and γ_2).

5. Adjustable carrier PWM

ACPWM uses two possible carrier signals in each sample period 'T_s', which are a rising toothed wave and a falling toothed wave. The wave which is used depends on the sign of the error. If the error is positive, the rising wave is used, and if the error is negative, the falling wave is used. Thus the switching period will be T_s or $2T_s$ depending on the sign of the error. Assuming a uniform distribution for the error, an average switching frequency can be defined as

$$f_{c,med} = \frac{3}{4} f_{ts}$$

Where f_{ts} is the frequency of the toothed saw wave. The RMS tracking error of current can be minimized using this conditional wave.

6. Simulation studies

A detailed simulation has been carried out for a simple GUPFC system consisting of two lines of 20 KV. The parameters of GUPFC system are given in Table 1. Two lines are feeding equal loads of 1MVA with 0.8 PF lagging. Phase-A of the supply voltage of lines L_1 and L_2 are shown in figure 10 (a) & (b). The effect of flicker in line L_2 is pronounced in line L_1 also. The series converter of GUPFC connected with lines L_1 and L_2 are operated in voltage flicker compensating mode. The compensated load voltage of lines L_1 and L_2 in figure 11 shows that load voltage tracks the desired reference accurately without RMS tracking error under ACPWM. It also proves the effectiveness of the two-neuron control technology for voltage flicker compensation. The degree of damping and dynamic performances is within the acceptable limits. The shunt converter is operated in power flow control mode which replenishes the dc-link energy storage. The dc-link voltage is presented in figure 12, which shows an initial drop at the start of GUPFC to compensate voltage flicker and is brought towards reference within a short time. The initial drop is due to sudden power change in line L_1 and initially, this power is supplied from the dc-link energy storage and the shunt controller takes a certain time to react to the change in energy. Thus the overall performance of the proposed method is satisfactory.

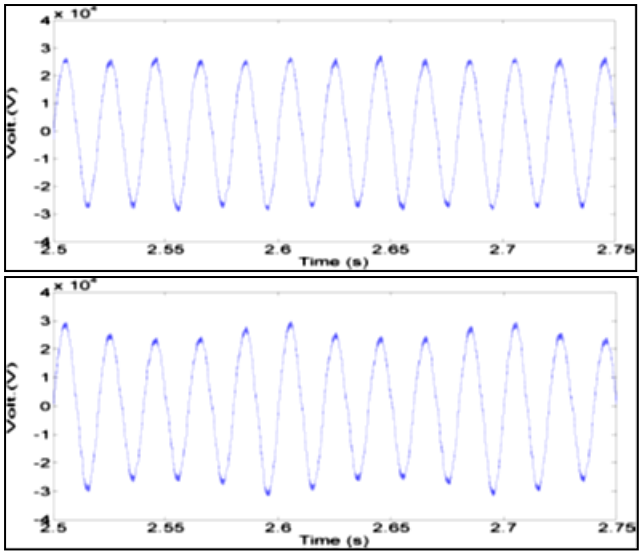

Fig.10 Uncompensated phase voltages of Lines L_1 and L_2

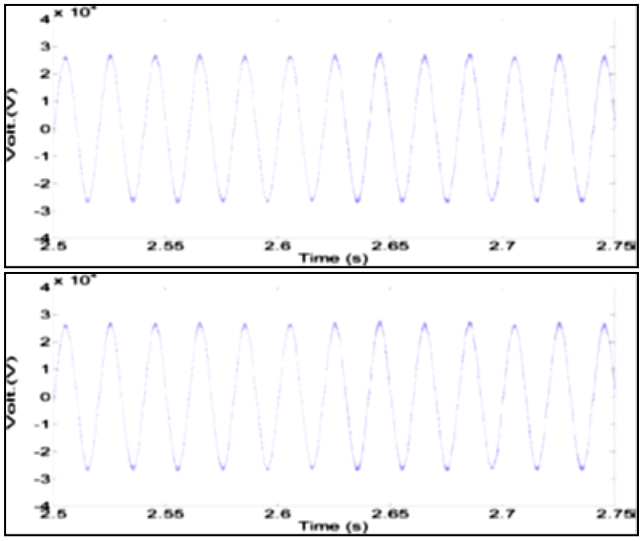

Fig. 11 Compensated phase voltages of Lines L_1 and L_2

Table 1 Parameters of the two-line GUPFC system

Parameter	Values
Supply voltage per phase (KV)	3.81
Load resistance (Ω)	35
Load inductance (mH)	83
Transformer resistance (Ω)	0.05
Transformer leakage inductance (mH)	1
Filter resistance (Ω)	0.05
Filter inductance (mH)	10
Filter capacitance (μF)	86
Common dc-link capacitance (μF)	14400

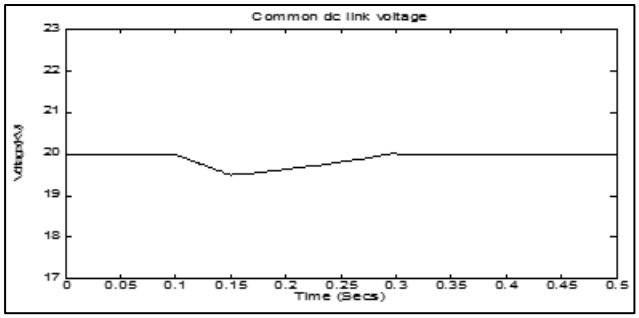

Fig. 12 Common dc-link voltages

7. Conclusion

The capability of any device used to compensate voltage flicker mainly depends on the amount of energy stored within the device. Moreover, the existing compensating devices cannot compensate flicker simultaneously all the lines under consideration. This work has proposed a new concept of using GUPFC in voltage flicker mitigation which can minimize the dc link energy storage, as well as, performs simultaneous compensation of all lines under consideration. Simulation results proved the efficiency of the proposed method. In the existing IDVR system, the amount of real power that a line can transfer to dc-link energy storage depends on the load PF. The proposed approach overcomes this limitation also. Thus this approach is a valuable contribution to the supply system in maintaining power quality. In future, this work can be extended for compensating more than two lines simultaneously.

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